

Specification for Approval

PRODUCT NAME: RGS10096064FR009
PRODUCT NO.: 9912801000

CUSTOMER
APPROVED BY
DATE:

RITDISPLAY CORP. APPROVED

REVISION RECORD

REV.	REVISION DESCRIPTION	REV. DATE	REMARK
X01	INITIAL RELEASE	2005. 12. 15	
X02	<ul style="list-style-type: none"> ■ Modify panel electrical specification ■ Modify reliability test conditions ■ Modify FPC layout 	2005. 12. 27	Page 8, 16 & 17
X03	<ul style="list-style-type: none"> ■ Modify lifetime specification ■ Modify CIE_x coordinate of green ■ Modify reliability test conditions ■ Modify protective film dimension 	2006. 01. 20	Page 6, 8, 16, 17 & 22
A01	<ul style="list-style-type: none"> ■ Add the information of module weight ■ Modify lifetime specification ■ Add the operating conditions for different luminance ■ Modify the D.C electrical characteristics ■ Modify the panel electrical specification – current, power consumption, luminance, CIE & contrast setting ■ Modify DC-DC circuit ■ Add the packing specification 	2006. 06. 20	Page 5, 6, 7, 8, 15 & 18
A02	<ul style="list-style-type: none"> ■ Modify specification of dark room contrast ■ Modify power on/off sequence ■ Modify packing specification 	2009. 03. 16	Page 4, 8, 13 & 18

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1. SCOPE

The purpose of this specification is to define the general provisions and quality requirements that apply to the supply of display cells manufactured by RiTdisplay. This document, together with the Module Assembly Drawing, is the highest-level specification for this product. It describes the product, identifies supporting documents and contains specifications, which are either not addressed, or are exceptions to the supporting documents.

2. WARRANTY

RiTdisplay warrants that the products delivered pursuant to this specification (or order) will conform to the agreed specifications for twelve (12) months from the shipping date ("Warranty Period"). RiTdisplay is obligated to repair or replace the products which are found to be defective or inconsistent with the specifications during the Warranty Period without charge, on condition that the products are stored or used as the conditions specified in the specifications. Nevertheless, RiTdisplay is not obligated to repair or replace the products without charge if the defects or inconsistency are caused by the force majeure or the reckless behaviors of the customer.

After the Warranty Period, all repairs or replacements of the products are subject to charge.

3. FEATURES

- Small molecular organic light emitting diode.
- Color : 65k Full colors
- Panel matrix : 96*3*64
- Driver IC : SSD1331Z
- Excellent Quick response time : 10 μ s
- Extremely thin thickness for best mechanism design : 1.45 mm
- High contrast : 2000:1
- Wide viewing angle : 160°
- Strong environmental resistance.
- 8-bit 6800-series Parallel Interface, 8-bit 8080-series Parallel Interface, Serial Peripheral.
- Wide range of operating temperature : -40 to 70°C

4. MECHANICAL DATA

NO	ITEM	SPECIFICATION	UNIT
1	Dot Matrix	96 (W) x (RxGxB) x 64 (H)	dot
2	Dot Size	0.057 (W) x 0.19 (H)	mm ²
3	Dot Pitch	0.07 (W) x 0.21 (H)	mm ²
4	Aperture Rate	74	%
5	Active Area	20.147 (W) x 13.42 (H)	mm ²
6	Panel Size	24.8 (W) x 22.42 (H)	mm ²
7	Panel Thickness	1.45 ± 0.1	mm
8	Module Size	24.8 (W) x 30.22 (H) x 1.45 (D)	mm ³
9	Diagonal A/A size	1.0	inch
10	Module Weight	1.69 ± 10%	gram

5. MAXIMUM RATING

ITEM	MIN	MAX	UNIT	Condition	Remark
Supply Voltage (V_{DD})	-0.3	3.5	V	$T_a = 25^{\circ}\text{C}$	IC maximum rating
Supply Voltage (V_{CC})	9	13.5	V	$T_a = 25^{\circ}\text{C}$	IC maximum rating
Operating Temp.	-40	70	$^{\circ}\text{C}$		
Storage Temp	-40	85	$^{\circ}\text{C}$		
Storage Humidity		85	%		
Life Time	13,000	-	Hrs	120 cd/m^2 , 50% checkerboard	Note (1)
Life Time	16,000	-	Hrs	100 cd/m^2 , 50% checkerboard	Note (2)
Life Time	20,000	-	Hrs	80 cd/m^2 , 50% checkerboard	Note (3)

Note:

(A) Under $V_{CC} = 13$ Volts, $T_a = 25^{\circ}\text{C}$, 50% RH.

(B) Life time is defined the amount of time when the luminance has decayed to less than 50% of the initial measured luminance.

(1) Setting of 120 cd/m^2 :

- Master contrast setting : 0x0DH
- Frame rate : 85 Hz
- Duty setting : 1/64

(2) Setting of 100 cd/m^2 :

- Master contrast setting : 0x0AH
- Frame rate : 85 Hz
- Duty setting : 1/64

(3) Setting of 80 cd/m^2 :

- Master contrast setting : 0x07H
- Frame rate : 85 Hz
- Duty setting : 1/64

6. ELECTRICAL CHARACTERISTICS

6.1 D.C ELECTRICAL CHARACTERISTICS

($V_{SS}=0V$, $V_{DD}=2.4$ to $3.5V$, $T_a=25^{\circ}C$)

SYMBOL	PARAMETERS	TEST CONDITION	MIN	TYP	MAX	UNIT
V_{CC}	Driver power supply (for OLED panel)	$T_a=-20^{\circ}C$ to $+60^{\circ}C$	12.5	13	13.5	V
V_{DD}	Operating voltage	$T_a=-20^{\circ}C$ to $+60^{\circ}C$	2.4	2.7	3.5	V
I_{DD}	Operating current for V_{DD}	$V_{DD}=2.7V$, $V_{CC}=11V$, Display ON, Contrast =FF, No panel attached	-	170	500	μA
I_{CC}	Operating current for V_{CC}	$V_{DD}=2.7V$, $V_{CC}=11V$, Display ON, Contrast =FF, No panel attached	-	700	1200	μA
V_{IH}	High logic input level	$I_{out}=100\mu A$, 3.3MHz	$0.8^* V_{DD}$	-	V_{DD}	V
V_{IL}	Low logic input level	$I_{out}=100\mu A$, 3.3MHz	0	-	$0.2^* V_{DD}$	V
V_{OH}	High logic output level	$I_{out}=100\mu A$, 3.3MHz	$0.9^* V_{DD}$	-	V_{DD}	V
V_{OL}	Low logic output level	$I_{out}=100\mu A$, 3.3MHz	0	-	$0.1^* V_{DD}$	V
I_{SEG}	Segment output current setting $V_{DD}=2.7V$, $V_{CC}=8V$, $I_{REF}=10\mu A$, All one pattern, Display on,	Contrast=FF	142	155	168	μA
		Contrast=7F	-	78	-	μA
		Contrast=3F	-	39	-	μA
		Contrast=1F	-	19	-	μA
		Contrast=0F	7	9	11	μA

Note 1: $V_{DD}=2.7V$; $V_{CC}= 13V$; Frame rate=85Hz ; No panel attached.

Note 2: The V_{CC} input must keep in a stable value; ripple and noise are not allowed.

6.2 ELECTRO-OPTICAL CHARACTERISTICS

PANEL ELECTRICAL SPECIFICATIONS

PARAMETER	MIN	TYP.	MAX	UNITS	COMMENTS
Normal mode current		16	18	mA	All pixels on (1)
Standby mode current		1	2	mA	Standby mode 10% pixels on (2)
Normal mode power consumption		208	234	mW	All pixels on (1)
Standby mode power consumption		13	26	mW	Standby mode 10% pixels on (2)
Normal mode Luminance	80	100		cd/m ²	Display Average
Standby mode Luminance		10		cd/m ²	
CIE _x (White)	0.24	0.28	0.32		x, y (CIE 1931)
CIE _y (White)	0.28	0.32	0.36		
CIE _x (Red)	0.61	0.65	0.69		
CIE _y (Red)	0.30	0.34	0.38		
CIE _x (Green)	0.21	0.25	0.29		
CIE _y (Green)	0.52	0.56	0.60		
CIE _x (Blue)	0.07	0.11	0.15		
CIE _y (Blue)	0.13	0.17	0.21		
Dark Room Contrast	2000:1				
Viewing Angle	160			degree	
Response Time		10		μs	

(1) Normal mode condition :

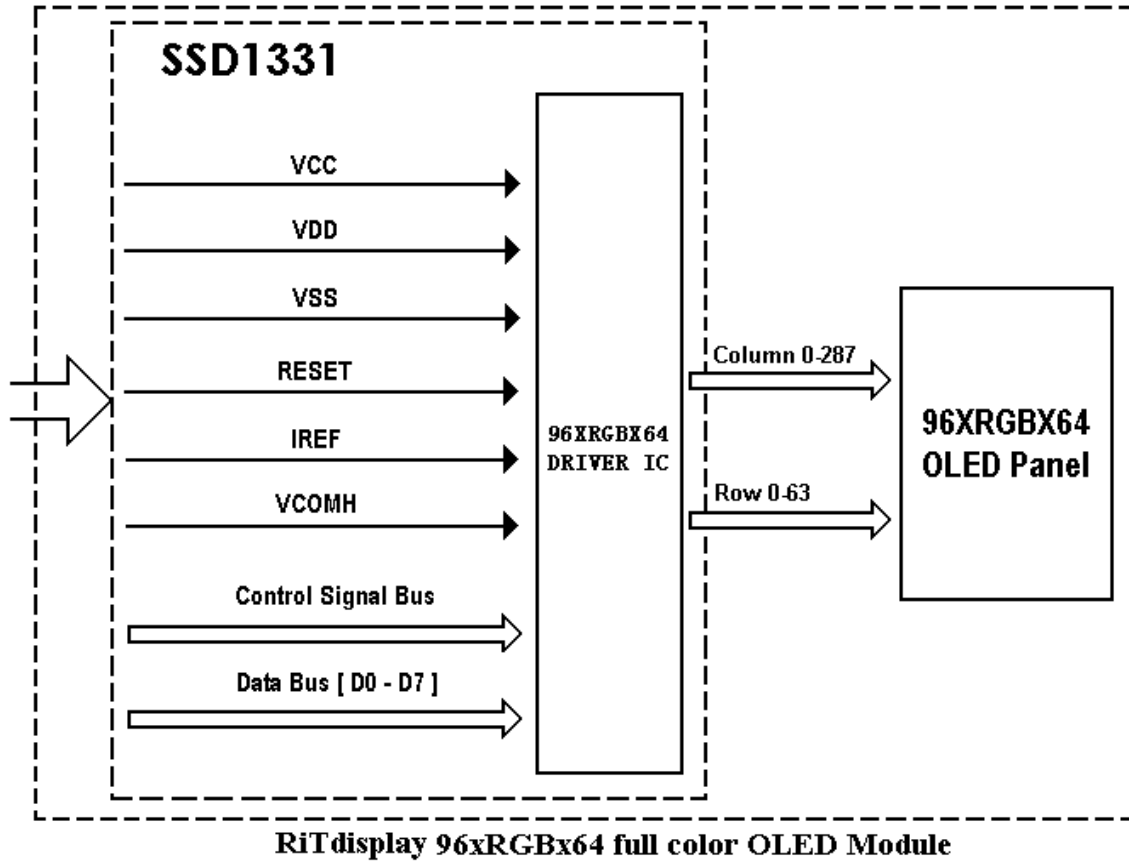
- Driving Voltage : 13 V
- Master contrast setting : 0x0AH
- Frame rate : 85 Hz
- Duty setting : 1/64

(2) Standby mode condition :

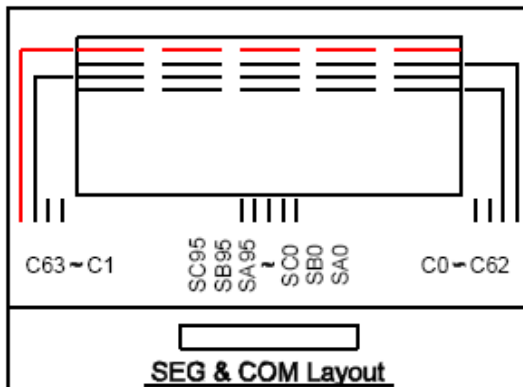
- Driving Voltage : 13V
- Master contrast setting : 0x01H
- Frame rate : 85 Hz
- Duty setting : 1/64

7. INTERFACE

7.1 FUNCTION BLOCK DIAGRAM



7.2 PANEL LAYOUT DIAGRAM



7.3 PIN ASSIGNMENTS

PIN NO	PIN NAME	TYPE	DESCRIPTION
1	NC	-	No connection.
2	VSS	I	Ground pin.
3	NC	-	No connection.
4	VCC	I	Positive high voltage power supply.
5	VCOMH	O	Com Voltage Output. A capacitor should be connected between this pin and V_{SS} .
6	D7	I/O	This pin is bi-direction data signal.
7	D6	I/O	This pin is bi-direction data signal.
8	D5	I/O	This pin is bi-direction data signal.
9	D4	I/O	This pin is bi-direction data signal.
10	D3	I/O	This pin is bi-direction data signal.
11	D2	I/O	This pin is bi-direction data signal.
12	D1	I/O	This pin is bi-direction data signal.
13	D0	I/O	This pin is bi-direction data signal.
14	E/RD#	I	MCU interface input. Data read operation is initiated when it's pull low.
15	R/W#	I	MCU interface input. Data write operation is initiated when it's pull low.
16	D/C#	I	Data/ command control. Pull high for write/read display data. Pull low for write command or read status.
17	RES#	I	Hardware reset signal. When it's low, initialization of SSD1331 is executed.
18	CS#	I	Chip select input ("Low" enable).
19	IREF	I	Reference current input pin. A resistor should be connected between this pin and V_{SS} .
20	BS2	I	MCU parallel interface selection input.
21	BS1	I	MCU parallel interface selection input.
22	VDD	I	Power supply for logic.
23	NC	-	No connection.
24	VCC	I	Positive high voltage power supply.
25	VDD	I	Power supply for logic.
26	VSS	I	Ground pin.
27	NC	-	No connection.

7.4 GRAPHIC DISPLAY DATA RAM ADDRESS MAP

The GDDRAM is a bit mapped static RAM holding the pattern to be displayed. The RAM size is 96 x 64 x 16bits.

For mechanical flexibility, re-mapping on both Segment and Common outputs can be selected by software. For vertical scrolling of the display, an internal register storing display start line can be set to control the portion of the RAM data to be mapped to the display.

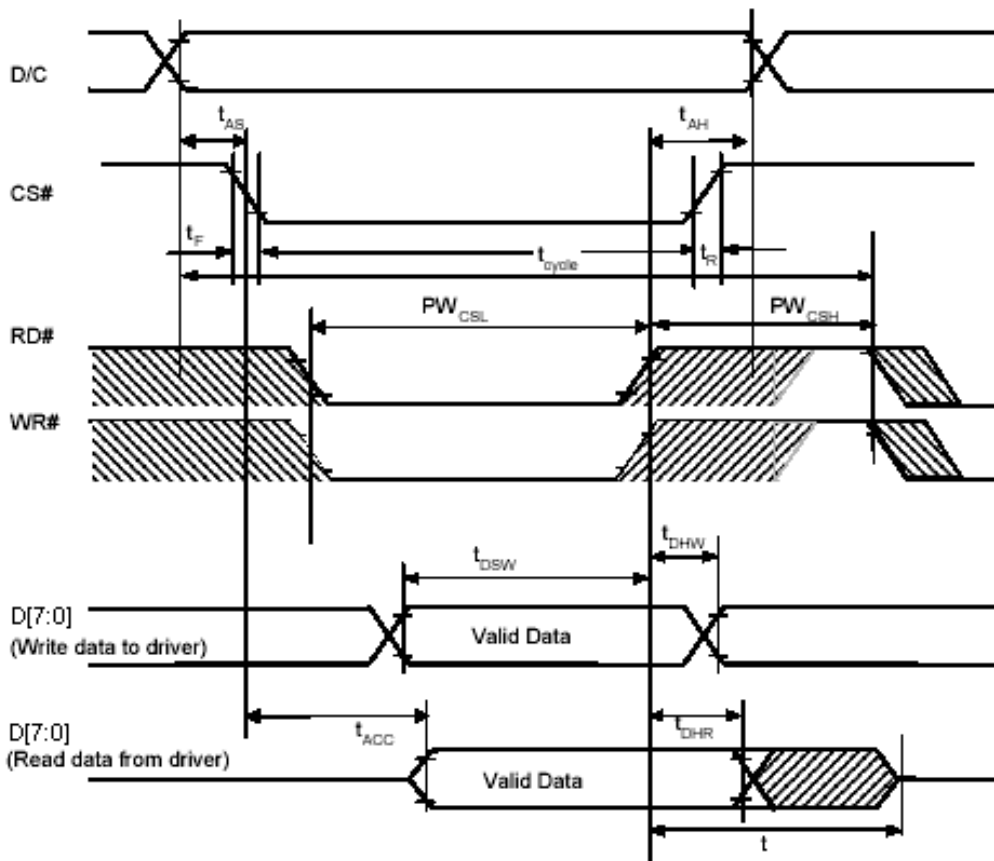
Each pixel has 16-bit data. Three sub-pixels for color A, B and C have 5 bits, 6 bits and 5 bits respectively. The arrangement of data pixel in graphic display data RAM is shown below.

Column Address	Normal	0	1	2	:	93	94	95													
	Remap	95	94	93	:	2	1	0													
Data Format		A4 B5 C4	A4 B5 C4	A4 B5 C4	:	A4 B5 C4	A4 B5 C4	A4 B5 C4													
		A3 B4 C3	A3 B4 C3	A3 B4 C3	:	A3 B4 C3	A3 B4 C3	A3 B4 C3													
		A2 B3 C2	A2 B3 C2	A2 B3 C2	:	A2 B3 C2	A2 B3 C2	A2 B3 C2													
		A1 B2 C1	A1 B2 C1	A1 B2 C1	:	A1 B2 C1	A1 B2 C1	A1 B2 C1													
		A0 B1 C0	A0 B1 C0	A0 B1 C0	:	A0 B1 C0	A0 B1 C0	A0 B1 C0													
Row Address		B0	B0	B0	:	B0	B0	B0													
Normal	Remap																				
0	63	5	6	5	5	6	5	5	6	5	:	5	6	5	5	6	5	5	6	5	
1	62										:										
2	61										:										
:	:	no. of bits of data in this cell																			
61	2										:										
62	1										:										
63	0										:										
SEG OUTPUT		SA0	SB0	SC0	SA1	SB1	SC1	SA2	SB2	SC2	:	SA93	SB93	SC93	SA94	SB94	SC94	SA95	SB95	SC95	
																	COM OUTPUT				
																	COM0				
																	COM1				
																	COM2				
																	:				
																	COM61				
																	COM62				
																	COM63				

7.5 INTERFACE TIMING CHART

($V_{DD}-V_{SS}=2.4$ to $3.5V$, $T_A=-40$ to $95^{\circ}C$)

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	300	-	-	ns
t_{AS}	Address Setup Time	0	-	-	ns
t_{AH}	Address Hold Time	0	-	-	ns
t_{DSW}	Write Data Setup Time	40	-	-	ns
t_{DHW}	Write Data Hold Time	15	-	-	ns
t_{DHR}	Read Data Hold Time	20	-	-	ns
t_{OH}	Output Disable Time	-	-	70	ns
t_{ACC}	Access Time	-	-	140	ns
PW_{CSL}	Chip Select Low Pulse Width (read)	120	-	-	ns
	Chip Select Low Pulse Width (write)	60	-	-	ns
PW_{CSH}	Chip Select High Pulse Width (read)	60	-	-	ns
	Chip Select High Pulse Width (write)	60	-	-	ns
t_R	Rise Time	-	-	15	ns
t_F	Fall Time	-	-	15	ns

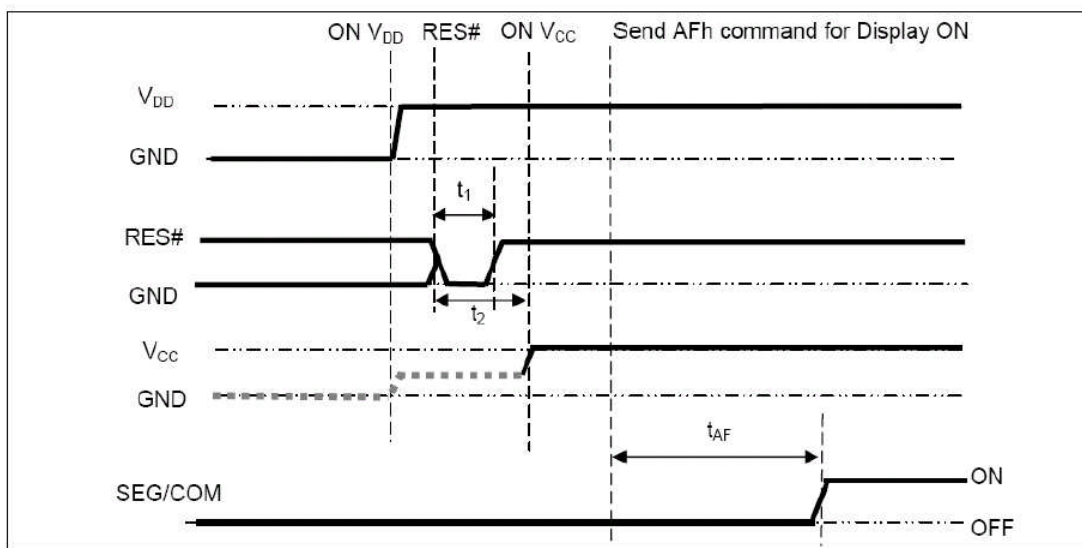


8. POWER ON / OFF SEQUENCE & APPLICATION CIRCUIT

8.1 POWER ON / OFF SEQUENCE

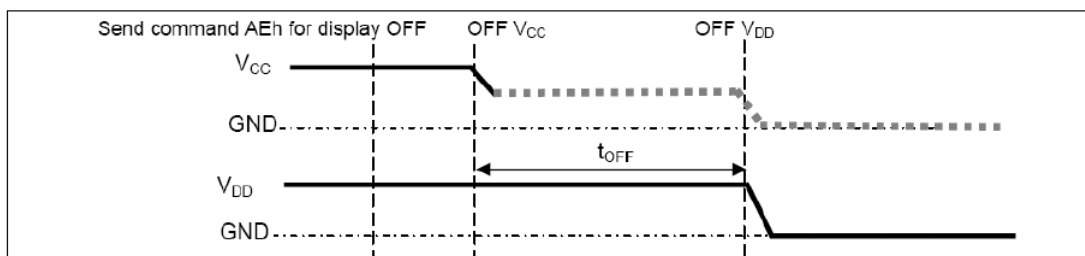
Power ON sequence:

1. Power ON V_{DD} .
2. After V_{DD} become stable, set RES# pin LOW (logic low) for at least $3\mu s(t_1)$ and then HIGH (logic high).
3. After set RES# pin LOW (logic low), wait for at least $3\mu s(t_2)$. Then Power ON V_{CC} .(1)
4. After V_{CC} become stable, send command AFh for display ON. SEG/COM will be ON after $100ms(t_{AF})$.



Power OFF sequence:

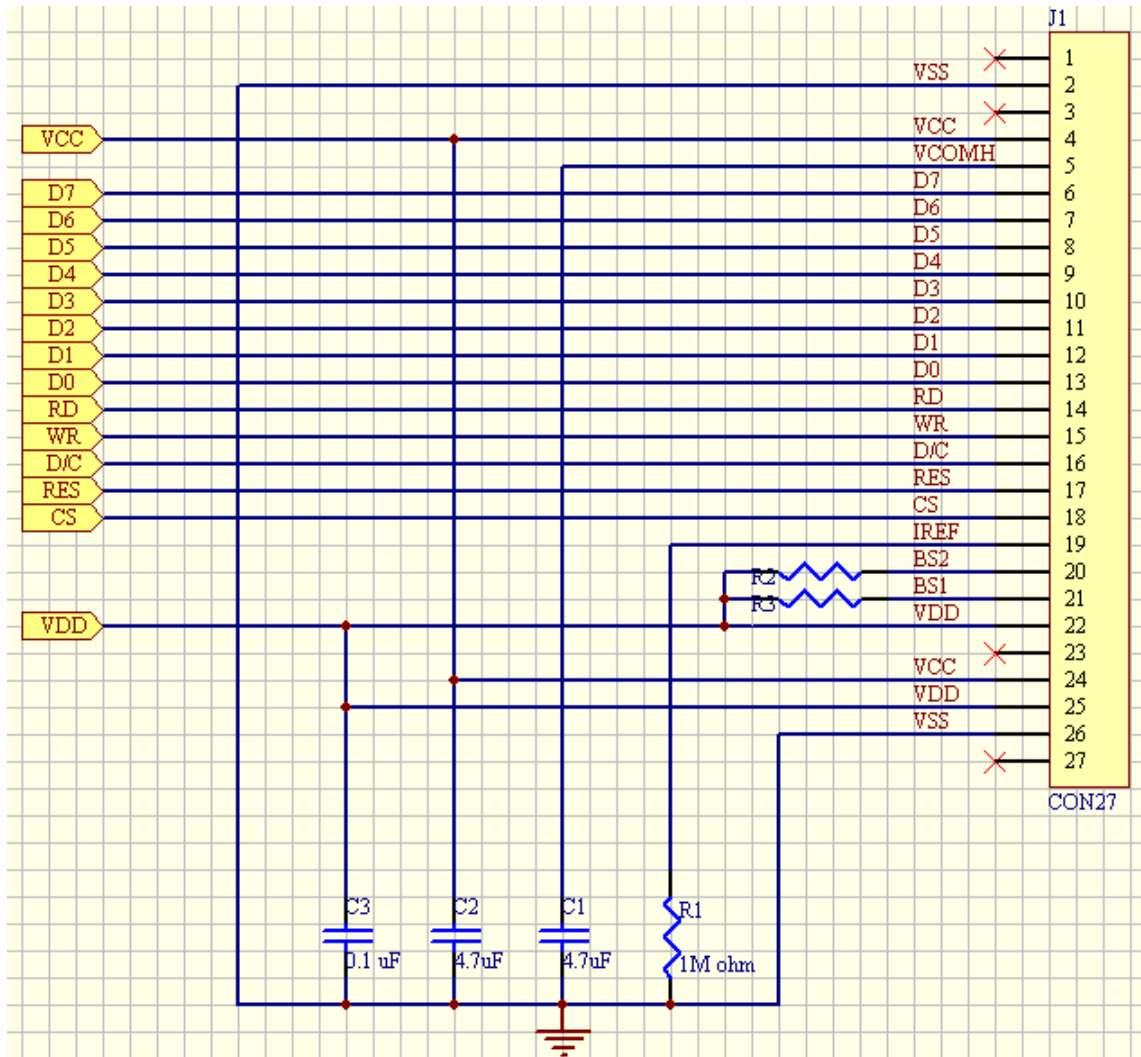
1. Send command AEh for display OFF.
2. Wait until panel discharges completely.
3. Power OFF V_{CC} . (1), (2)
4. Wait for t_{OFF} . Power OFF V_{DD} . (where Minimum $t_{OFF}=80ms$, Typical $t_{OFF}=100ms$)



Note:

- (1) Since an ESD protection circuit is connected between V_{DD} and V_{CC} , V_{CC} becomes lower than V_{DD} whenever V_{DD} is ON and V_{CC} is OFF as shown in the dotted line of V_{CC} in above figures.
- (2) V_{CC} should be disabled when it is OFF.

8.2 APPLICATION CIRCUIT



Recommend components:

The C1 and C2: 4.7uF (0805) / 16V

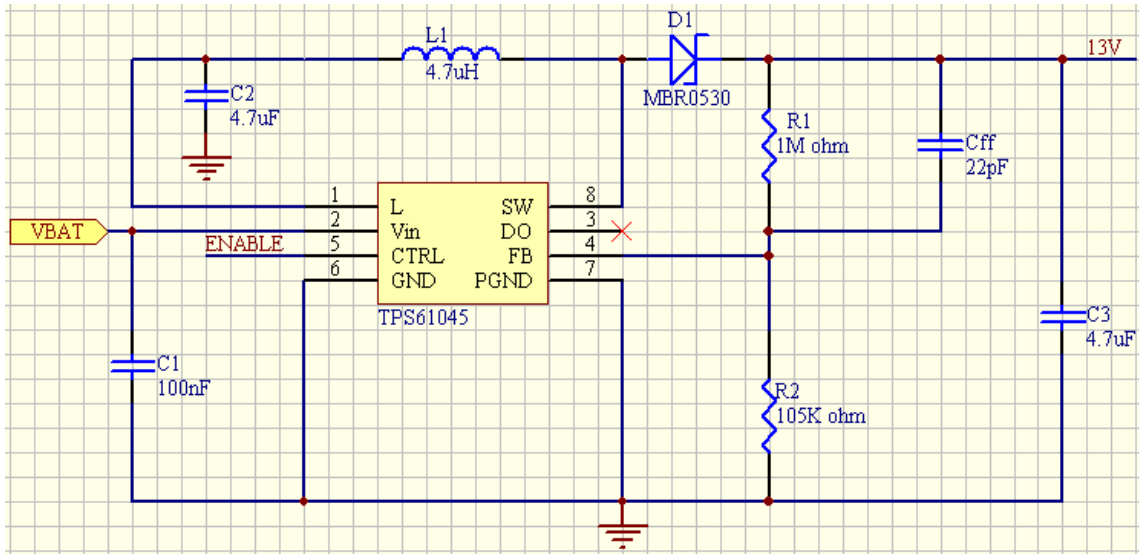
The C3: 0.1uF (0603) / 16V

The R1: 1M ohm (0603), 1%

The R2 & R3: Pull high resistor 10K ohm, or connect to VDD directly.

This circuit is designed for 8080 interface.

DC-DC Circuit



Customer should tune the R1 and R2 value.

(The value of each component can refer to tps61045 IC datasheet)

8.3 COMMAND TABLE

Refer to IC Spec.: SSD1331

9. RELIABILITY TEST CONDITIONS

No.	Items	Specification	Quantity
1	High temp. (Non-operation)	85°C, 240hrs	5
2	High temp. (Operation)	70°C, 120hrs	5
3	Low temp. (Operation)	-40°C, 120hrs	5
4	High temp. / High humidity (Operation)	65°C, 90%RH, 120hrs	5
5	Thermal shock (Non-operation)	-40°C ~85°C (-40°C /30min; transit /3min; 85°C /30min; transit /3min) 1cycle: 66min, 20 cycles	5
6	Vibration	Frequency : 5~50HZ, 0.5G Scan rate : 1 oct/min Time : 2 hrs/axis Test axis : X, Y, Z	1 Carton
7	Drop	Height: 120cm Sequence : 1 angle 、 3 edges and 6 faces Cycles: 1	1 Carton
8	ESD (Non-operation)	Air discharge model, ±8kV, 10 times	5

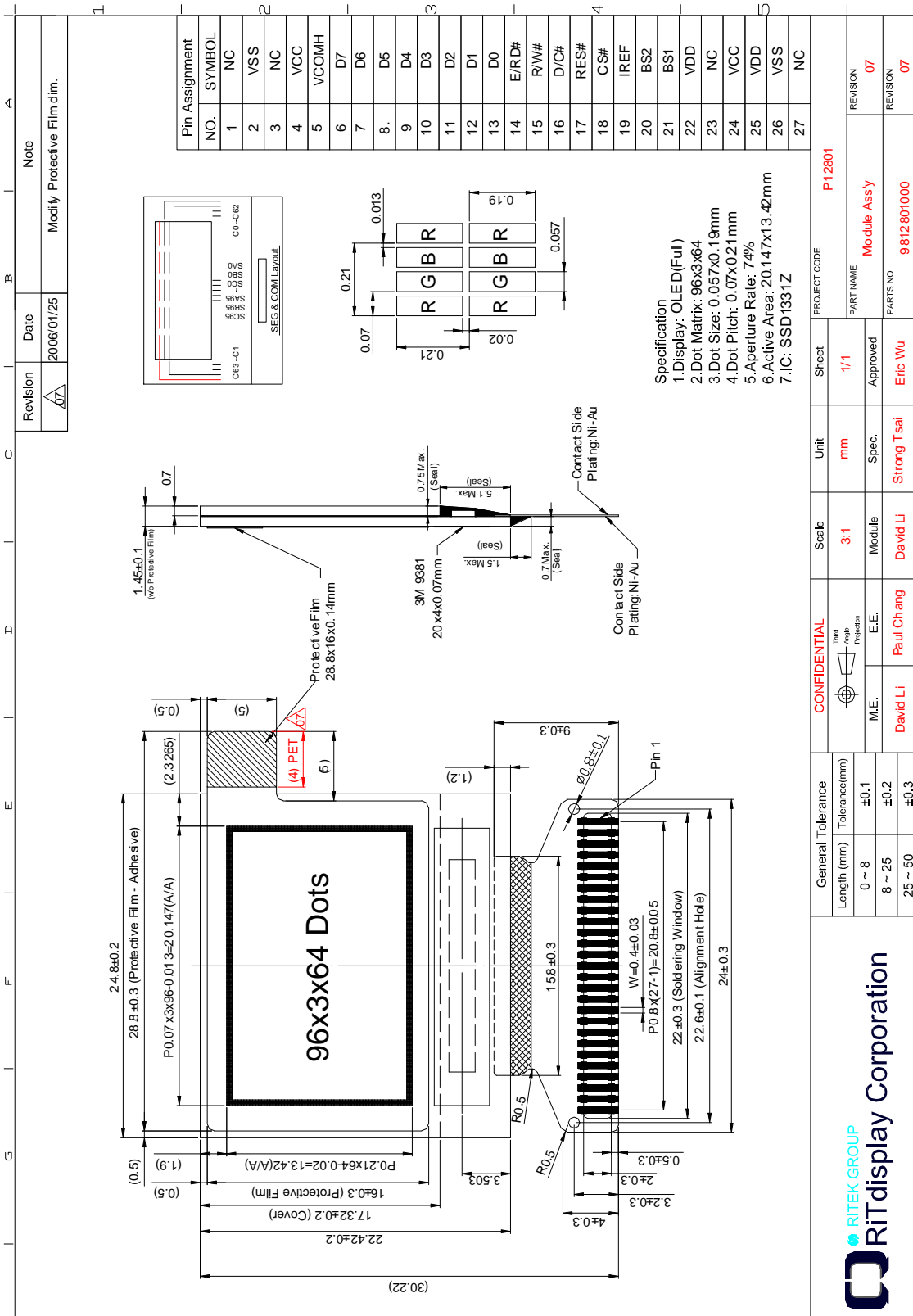
Test and measurement conditions

1. All measurements shall not be started until the specimens attain to temperature stability.
2. All-pixels-on is used as operation test pattern.

Evaluation criteria

1. The function test is OK.
2. No observable defects.
3. Luminance: > 50% of initial value.
4. Current consumption: within \pm 50% of initial value.

10. EXTERNAL DIMENSION



11. PACKING SPECIFICATION

Revision	Date	Note
A02	2009/03/06	Revised package quantity

① P12801 Module
P/N: 9812801000
Face Down, Rotate packing
面朝下, 旋轉放置

② Packing Tray
P/N: 3008000069
330x270x11.7mm, t=0.7mm

③ EPE Cover Foam
P/N: 3002000092
281.4x227.4x2mm

④ 5G Silica Gel Desiccants
- 5G 矽膠乾燥劑
P/N: 3010000002

⑤ Vacuum Bag ONYILDPE
真空包裝袋 ONYILDPE
P/N: 3003000012
480x285x90mm
Vacuum Packing, 4 sec
抽真空4秒

⑥ Antistatic Bubble Bag
抗靜電氣泡袋
P/N: 3003000016
440x(350+450)mm

⑦ Pizza Box
P/N: 3001000005
345x285x88, B 級
B Corrugated

⑧ 藍色 Carton
Carton
P/N: 3000000012
597x385x290mm

⑨ Label
標籤
P/N: 3006000000
x1 pcs

⑩ Tape
封膠帶
P/N: 3208000125

① x 1 pcs (empty)

② x 1 pcs

③ x 1 pcs

④ x 4

⑤ x 10 pcs

⑥ x 9 pcs

⑦ x 6 pcs

⑧ x 1 pcs

⑨ x 6 pcs

⑩ x 6 pcs

Item	Part No.	Description	QTY
1	9812801000	P12801 Module Assy	1296
2	3008000069	Tray 330x270x11.7mm PET t=0.7mm	60
3	3002000092	EPE Cover Foam 281.4x227.4x2mm	108
4	3010000002	5G Silica Gel Desiccants	24
5	3003000012	Vacuum Bag 480x285x90mm	6
6	3003000016	Antistatic Bubble Bag 440x(350+450)mm	6
7	3001000005	Pizza Box 345x285x88, B Corrugated	6
8	3000000012	Carton, 597x385x290mm	1
9	3006000000	Label	7
10	3208000125	Tape	6

General Tolerance		Scale		PROJECT CODE	
Length (mm)	Tolerance(mm)	1:9	mm	P12801	Sheet
0 ~ 8	±0.1	M.E.	Spec.	Approved	1/1
8 ~ 25	±0.2	M.E.	Module	Strong Tsai	REVISION
25 ~ 50	±0.3	M.E.	Valerie Lo	02	02
		M.E.	Irene Fan	PARTS NO.	
		M.E.	9912801000	PART NAME	
		M.E.	Packing Tray Instruction	REVISION	
		M.E.	02	02	

12. APPENDIXES

APPENDIX 1: DEFINITIONS

A. DEFINITION OF CHROMATICITY COORDINATE

The chromaticity coordinate is defined as the coordinate value on the CIE 1931 color chart for R, G, B, W.

B. DEFINITION OF CONTRAST RATIO

The contrast ratio is defined as the following formula:

$$\text{Contrast Ratio} = \frac{\text{Luminance of all pixels on measurement}}{\text{Luminance of all pixels off measurement}}$$

C. DEFINITION OF RESPONSE TIME

The definition of turn-on response time T_r is the time interval between a pixel reaching 10% of steady state luminance and 90% of steady state luminance. The definition of turn-off response time T_f is the time interval between a pixel reaching 90% of steady state luminance and 10% of steady state luminance. It is shown in Figure 2.

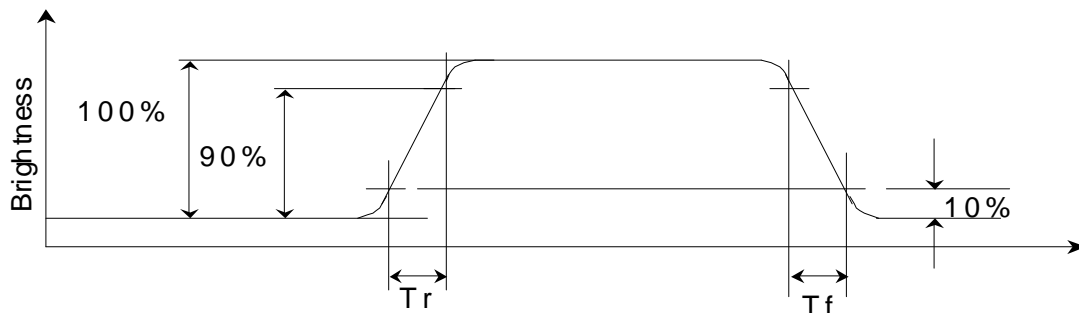


Figure 2 Response time

D. DEFINITION OF VIEWING ANGLE

The viewing angle is defined as Figure 3. Horizontal and vertical (H & V) angles are determined for viewing directions where luminance varies by 50% of the perpendicular value.

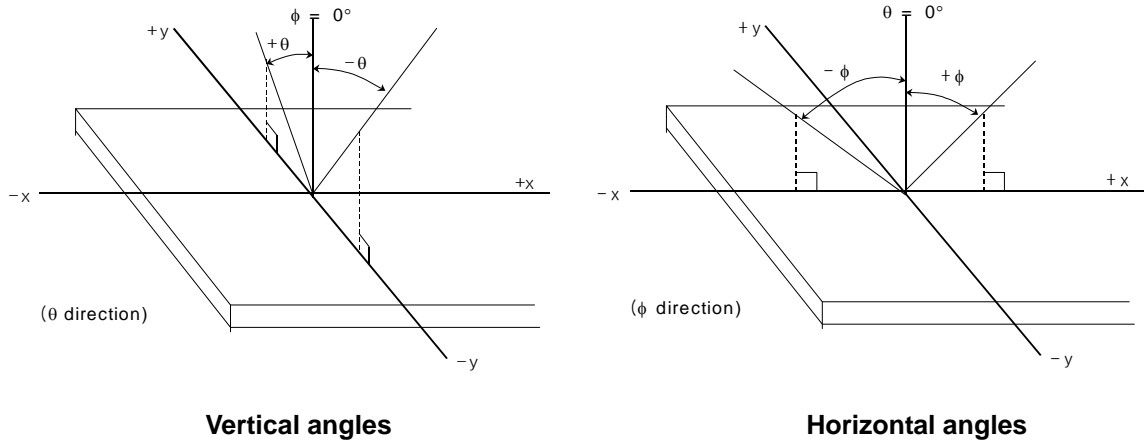
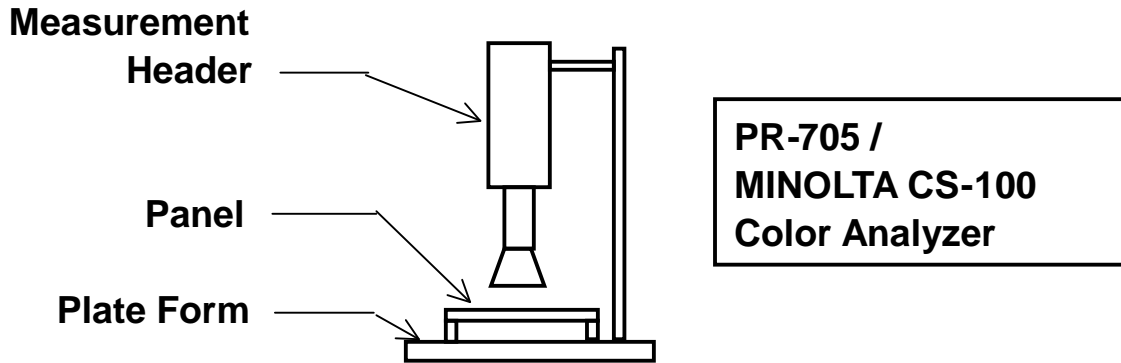


Figure 3 Viewing Angle

APPENDIX 2: MEASUREMENT APPARATUS

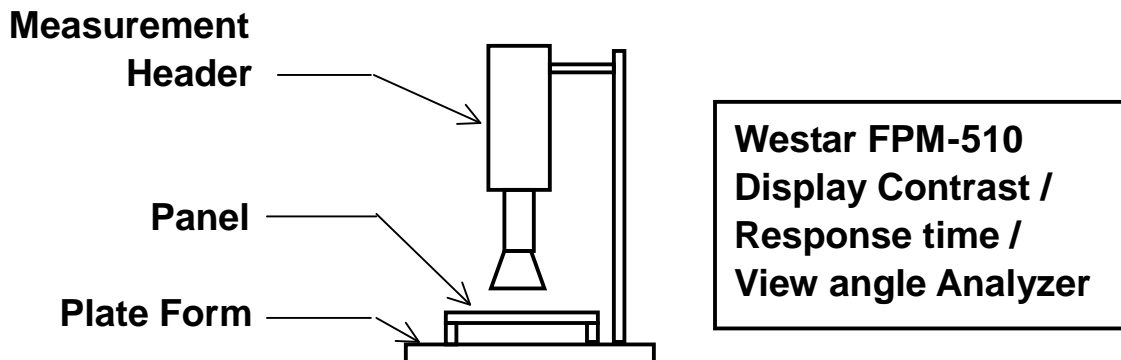
A. LUMINANCE/COLOR COORDINATE

PHOTO RESEARCH PR-705, MINOLTA CS-100

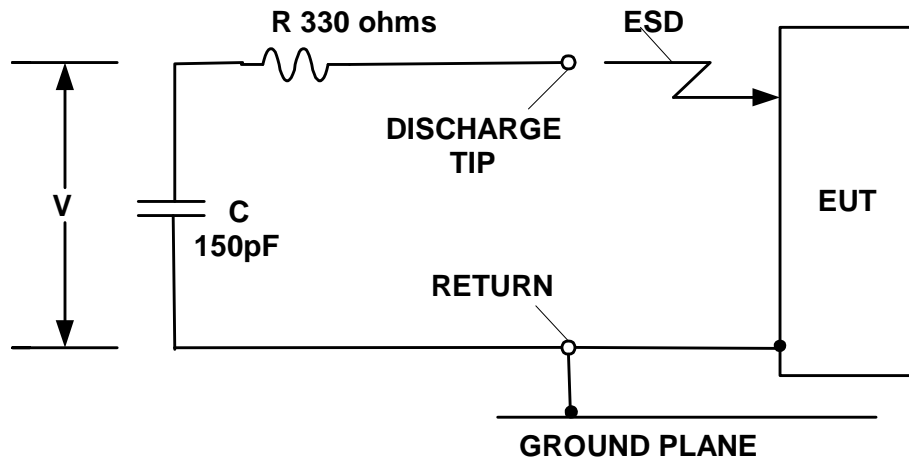


B. CONTRAST / RESPONSE TIME / VIEWING ANGLE

WESTAR CORPORATION FPM-510



C. ESD ON AIR DISCHARGE MODE



APPENDIX 3: PRECAUTIONS

A. RESIDUE IMAGE

Because the pixels are lighted in different time, the luminance of active pixels may reduce or differ from inactive pixels. Therefore, the residue image will occur. To avoid the residue image, every pixel needs to be lighted up uniformly.