Specification for Approval

PRODUCT NAME: **RGS10128032WR000**
PRODUCT NO.: **9917501000**

CUSTOMER
APPROVED BY
DATE:

RITDISPLAY CORP. APPROVED

REVISION RECORD

REV.	REVISION DESCRIPTION	REV. DATE	REMARK
X01	INITIAL RELEASE	2007. 01. 11	
X02	■ Add the operating conditions for different luminance ■ Add the panel electrical specifications – current, power consumption, standby mode luminance, driving voltage & contrast setting ■ Modify tape size	2007. 03. 01	Page 6, 7, 8 & 16
A01	■ Add the information of module weight ■ Modify D.C electrical characteristics ■ Modify power on/off sequence ■ Add the packing specification	2007. 05. 16	Page 5, 7, 13 & 17

CONTENTS

ITEM	PAGE
1. SCOPE	4
2. WARRANTY	4
3. FEATURES	4
4. MECHANICAL DATA	5
5. MAXIMUM RATINGS	6
6. ELECTRICAL CHARACTERISTICS	7
6.1 D.C ELECTRICAL CHARACTERISTICS	
6.2 ELECTRO-OPTICAL CHARACTERISTICS	
7. INTERFACE	9
7.1 FUNCTION BLOCK DIAGRAM	
7.2 PANEL LAYOUT DIAGRAM	
7.3 PIN ASSIGNMENTS	
7.4 GRAPHIC DISPLAY DATA RAM ADDRESS MAP	
7.5 INTERFACE TIMING CHART	
8. POWER ON / OFF SEQUENCE & APPLICATION CIRCUIT	13
8.1 POWER ON / OFF SEQUENCE	
8.2 APPLICATION CIRCUIT	
8.3 COMMAND TABLE	
9. RELIABILITY TEST CONDITIONS	15
10. EXTERNAL DIMENSION	16
11. PACKING SPECIFICATION	17
12. APPENDIXES	18

1. SCOPE

The purpose of this specification is to define the general provisions and quality requirements that apply to the supply of display cells manufactured by RiTdisplay. This document, together with the Module Ass'y Drawing, is the highest-level specification for this product. It describes the product, identifies supporting documents and contains specifications.

2. WARRANTY

RiTdisplay warrants that the products delivered pursuant to this specification (or order) will conform to the agreed specifications for twelve (12) months from the shipping date ("Warranty Period"). RiTdisplay is obligated to repair or replace the products which are found to be defective or inconsistent with the specifications during the Warranty Period without charge, on condition that the products are stored or used as the conditions specified in the specifications. Nevertheless, RiTdisplay is not obligated to repair or replace the products without charge if the defects or inconsistency are caused by the force majeure or the reckless behaviors of the customer.
After the Warranty Period, all repairs or replacements of the products are subject to charge.

3. FEATURES

- Small molecular organic light emission diode
- Color : White
- Panel matrix : 128*32
- Driver IC : SSD1305
- Excellent quick response time.
- Extremely thin thickness for best mechanism design : 1.61mm
- High contrast : 2000:1
- Wide viewing angle : 160°
- Serial Peripheral Interface.
- Wide range of operating temperature : -40 to 70 °C
- Anti-glare polarizer.

4. MECHANICAL DATA

NO	ITEM	SPECIFICATION	UNIT
1	Dot Matrix	128 (W) x 32 (H)	dot
2	Dot Size	0.18 (W) x 0.18 (H)	mm^2
3	Dot Pitch	0.20 (W) x 0.20 (H)	mm^2
4	Aperture Rate	81	%
5	Active Area	25.58 (W) x 6.38 (H)	mm^2
6	Panel Size	30.4 (W) x 14.5 (H)	mm^2
7	Panel Thickness	1.61 ± 0.1	mm
8	Module Size	30.4 (W) x 34.5 (H) x 1.61 (D)	mm^3
9	Diagonal A/A size	1.0	inch
10	Module Weight	1.43 ± 10%	gram

5. MAXIMUM RATINGS

ITEM	MIN	MAX	UNIT	Condition	Remark
Supply Voltage (V_{DD})	-0.3	3.5	V	Ta = 25°C	IC maximum rating
Supply Voltage (Vcc)	8	16	V	Ta = 25°C	IC maximum rating
Operating Temp.	-40	70	°C		
Storage Temp	-40	85	°C		
Humidity	-	85	%		
Life Time	21,000	-	Hrs	140cd/m^2, 50% checkerboard	Note (1)
Life Time	25,000		Hrs	120 cd/m^2, 50% checkerboard	Note (2)
Life Time	30,000	-	Hrs	100 cd/m^2, 50% checkerboard	Note (3)

Note:

(A) Under Vcc = 12V, Ta = 25°C, 50% RH.

(B) Life time is defined the amount of time when the luminance has decayed to less than 50% of the initial measured luminance.

(1) Setting of 140 cd/m^2 :

- Contrast setting : 0x4C
- Frame rate : 105Hz
- Duty setting : 1/32

(2) Setting of 120 cd/m^2 :

- Contrast setting : 0x42
- Frame rate : 105Hz
- Duty setting : 1/32

(3) Setting of 100 cd/m^2 :

- Contrast setting : 0x33
- Frame rate : 105Hz
- Duty setting : 1/32

6. ELECTRICAL CHARACTERISTICS

6.1 D.C ELECTRICAL CHARACTERISTICS

(V_{SS}=0V, V_{DD}=2.4 to 3.5V, Ta=25°C)

SYMBOL	PARAMETERS	TEST CONDITION	MIN	TYP	MAX	UNIT
V_{CC}	Analog power supply (for OLED panel)		11.5	12	12.5	V
V_{DD}	Digital power supply		2.4	2.7	3.5	V
V_{DDIO}	Power supply for I/O pins		1.6	-	V_{DD}	V
I_{DD}	Operating current for V_{DD} V_{DD} = 2.7V, V_{CC} = 12V, IREF = 10uA No loading, All Display ON	Contrast=FF	-	100	-	uA
I_{CC}	Operating current for V_{CC} V_{DD} = 2.7V, V_{CC} = 12V, IREF = 10uA, No loading, All Display ON	Contrast=FF	-	550	-	uA
V_{IH}	Hi logic input level		0.8* V_{DDIO}	-	V_{DDIO}	V
V_{IL}	Low logic input level		0	-	0.2* V_{DDIO}	V
V_{OH}	Hi logic output level		0.9* V_{DDIO}	-	V_{DDIO}	V
V_{OL}	Low logic output level		0	-	0.1* V_{DDIO}	V
I_{SEG}	Segment on output current V_{DD}=2.7V, V_{CC}=12V, IREF=10uA, Display on, Segment pin under test is connected with a 20K resistive load to V_{SS}	Contrast=FF	294	320	346	uA
		Contrast=AF	-	220	-	uA
		Contrast=7F	-	159	-	uA
		Contrast=3F	-	79	-	uA
		Contrast=0F	-	19	-	uA

Note 1: V_{DD}=2.7V ; V_{CC}= 12V ; Frame rate=105Hz ; No panel attached.

Note 2: The Vcc input must keep in a stable value; ripple and noise are not allowed.

6.2 ELECTRO-OPTICAL CHARACTERISTICS

PANEL ELECTRICAL SPECIFICATIONS

PARAMETER	MIN	TYP.	MAX	UNITS	COMMENTS
Normal mode current		6	7	mA	All pixels on (1)
Standby mode current		1	2	mA	Standby mode 10% pixels on (2)
Normal mode power consumption		72	84	mW	All pixels on (1)
Standby mode power consumption		12	24	mW	Standby mode 10% pixels on (2)
Normal Luminance	100	120		cd/m^2	Display Average
Standby Luminance		20		cd/m^2	Display Average
CIEx (White)	0.24	0.28	0.32		x, y (CIE 1931)
CIEy (White)	0.28	0.32	0.36		
Dark Room Contrast	2000:1				
Viewing Angle	160			degree	
Response Time		10		μs	

(1) Normal mode condition :

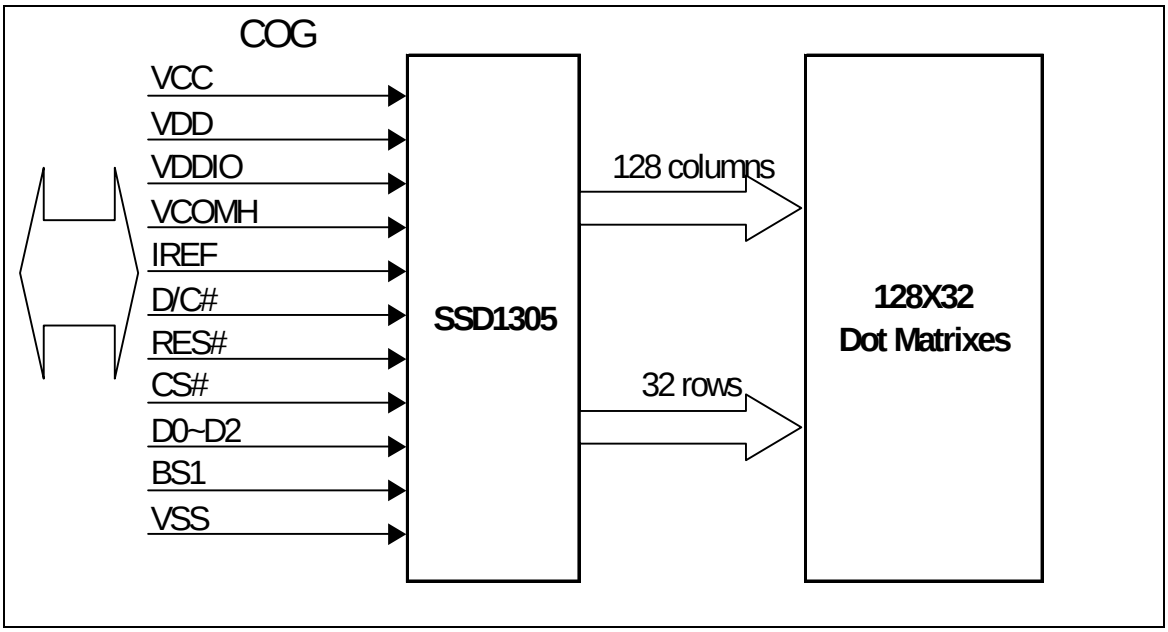
- Driving Voltage : 12V
- Contrast setting : 0x42
- Frame rate : 105Hz
- Duty setting : 1/32

(2) Standby mode condition :

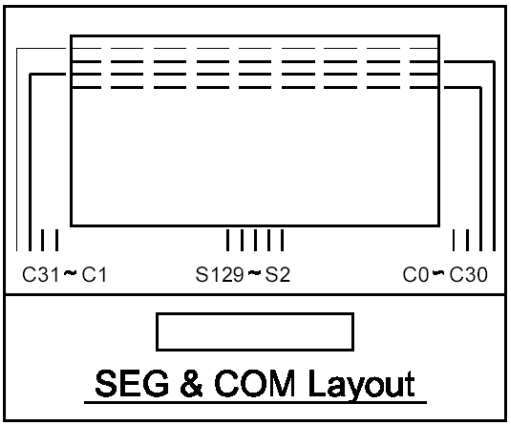
- Driving Voltage : 12V
- Contrast setting : 0x05
- Frame rate : 105Hz
- Duty setting : 1/32

7. INTERFACE

7.1 FUNCTION BLOCK DIAGRAM



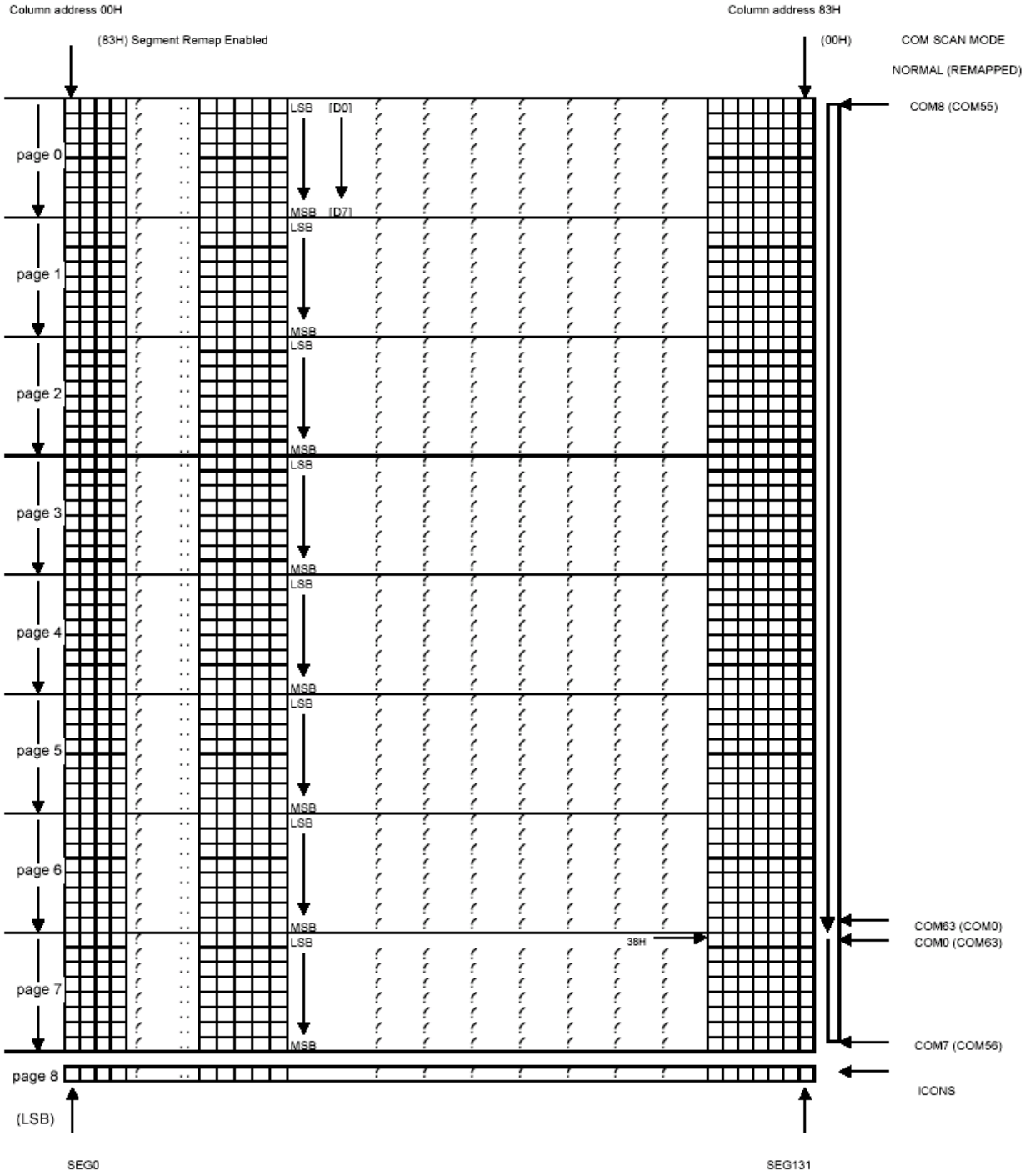
7.2 PANEL LAYOUT DIAGRAM



7.3 PIN ASSIGNMENTS

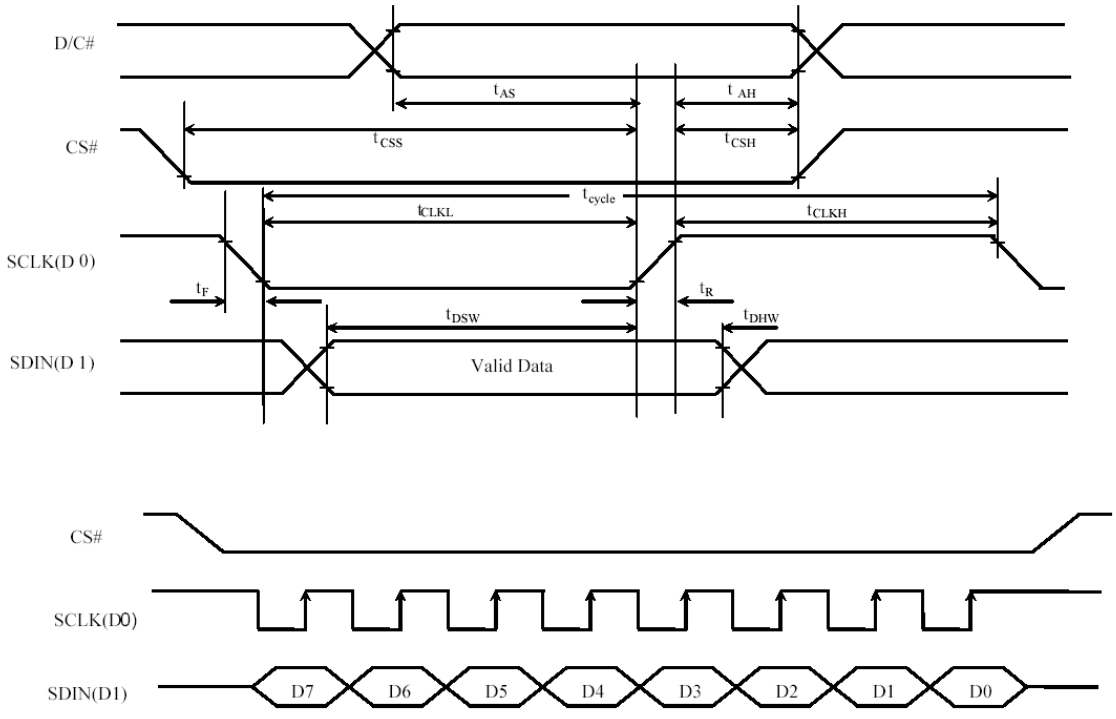
PIN NAME	PIN NO	DESCRIPTION
NC	1	No connection.
VSS	2	Ground.
VCC	3	Power supply for analog circuit.
VCOMH	4	Com Voltage Output. A capacitor should be connected between this pin and V_{SS}.
IREF	5	Reference current input pin. A resistor should be connected between this pin and V_{SS}.
D2	6	In SPI application, the pin should be floated.
D1	7	Data bus(SDIN)
D0	8	Data bus(SCLK)
D/C#	9	Data/ Command control. Pull high for write/read display data. Pull low for write command or read status.
RES#	10	Reset signal input. When it's low, initialization of SSD1305 is executed.
CS#	11	Chip select input.
BS1	12	Interface select pin. SPI: Active Low.
VDDIO	13	This pin is a power supply pin of I/O buffer.
VDD	14	Power supply for logic circuit.
VSS	15	Ground.
NC	16	No connection.

7.4 GRAPHIC DISPLAY DATA RAM ADDRESS MAP



7.5 INTERFACE TIMING CHART

Symbol	Parameter	Min	Typ	Max	Unit
t_{cycle}	Clock Cycle Time	250	-	-	ns
t_{AS}	Address Setup Time	150	-	-	ns
t_{AH}	Address Hold Time	150	-	-	ns
t_{CSS}	Chip Select Setup Time	120	-	-	ns
t_{CSH}	Chip Select Hold Time	60	-	-	ns
t_{DSW}	Write Data Setup Time	50	-	-	ns
t_{DHW}	Write Data Hold Time	15	-	-	ns
t_{CLKL}	Clock Low Time	100	-	-	ns
t_{CLKH}	Clock High Time	100	-	-	ns
t_R	Rise Time	-	-	15	ns
t_F	Fall Time	-	-	15	ns

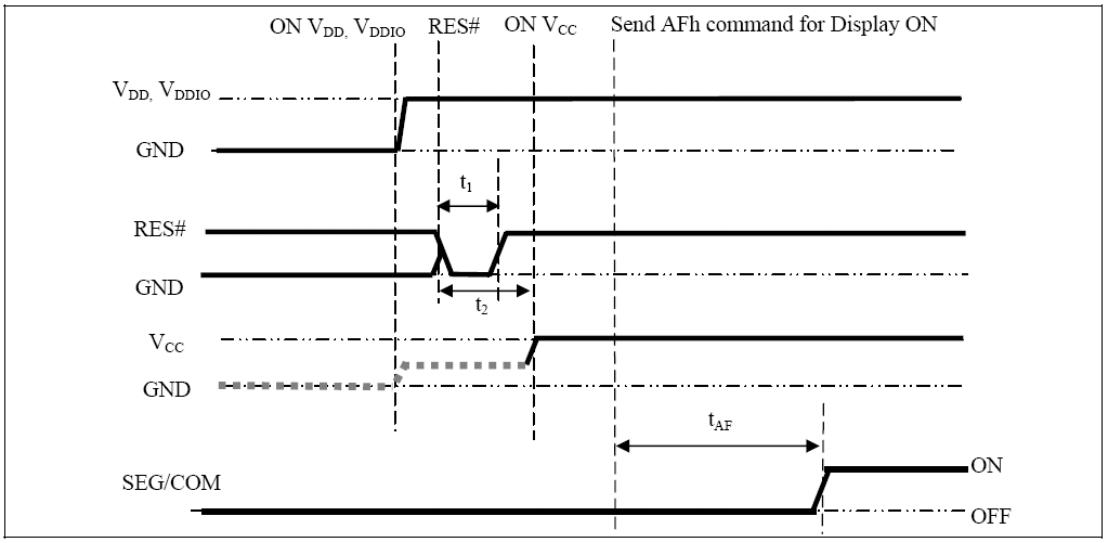


8. POWER ON / OFF SEQUENCE & APPLICATION CIRCUIT

8.1 POWER ON / OFF SEQUENCE

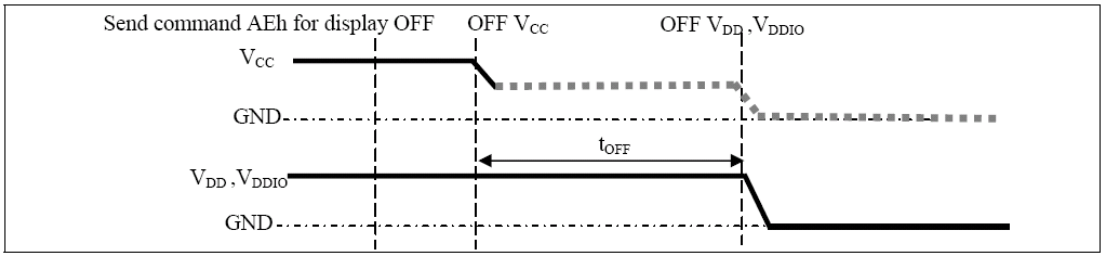
Power ON sequence:

1. Power ON V_{DD}, V_{DDIO}.
2. After V_{DD}, V_{DDIO} become stable, set RES# pin LOW (logic low) for at least 3us(t_1) and then HIGH (logic high).
3. After set RES# pin LOW (logic low), wait for at least 3us(t_2).Then Power ON V_{CC}.(1)
4. After V_{CC} become stable, send command AFh for display ON. SEG/COM will be ON after 100ms(t_{AF}).



Power OFF sequence:

1. Send command AEh for display OFF.
2. Power OFF V_{CC}. (1), (2)
3. Wait for t_{OFF}. Power OFF V_{DD}, V_{DDIO}. (where Minimum t_{OFF}=0ms, Typical t_{OFF}=100ms)

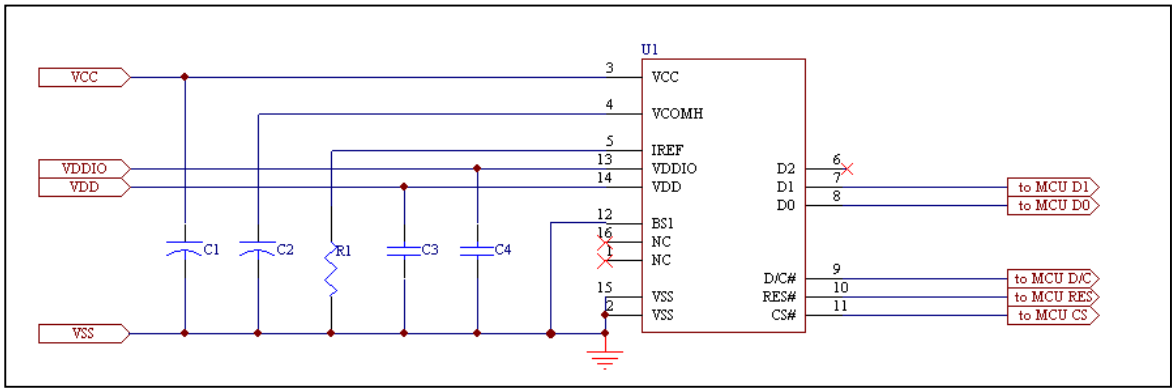


Note:

(1) Since an ESD protection circuit is connected between V_{DD}, V_{DDIO} and V_{CC}, V_{CC} becomes lower than V_{DD} whenever V_{DD}, V_{DDIO} is ON and V_{CC} is OFF as shown in the dotted line of V_{CC} in above figures.

(2) V_{CC} should be disabled when it is OFF.

8.2 APPLICATION CIRCUIT



VDDIO must always be equal or lower than VDD.

8.3 COMMAND TABLE

Refer to SSD1305 IC Spec.

9. RELIABILITY TEST CONDITIONS

No.	Items	Specification	Quantity
1	High temp. (Non-operation)	85°C, 240hrs	5
2	High temp. (Operation)	70°C, 120hrs	5
3	Low temp. (Operation)	-40°C, 120hrs	5
4	High temp. / High humidity (Operation)	65°C, 90%RH, 120hrs	5
5	Thermal shock (Non-operation)	-40°C ~85°C (-40°C /30min; transit /3min; 85°C /30min; transit /3min) 1cycle: 66min, 100 cycles	5
6	Vibration	Frequency : 5~50HZ, 0.5G Scan rate : 1 oct/min Time : 2 hrs/axis Test axis : X, Y, Z	1 Carton
7	Drop	Height: 120cm Sequence : 1 angle、3 edges and 6 faces Cycles: 1	1 Carton
8	ESD (Non-operation)	Air discharge model, ±8kV, 10 times	5

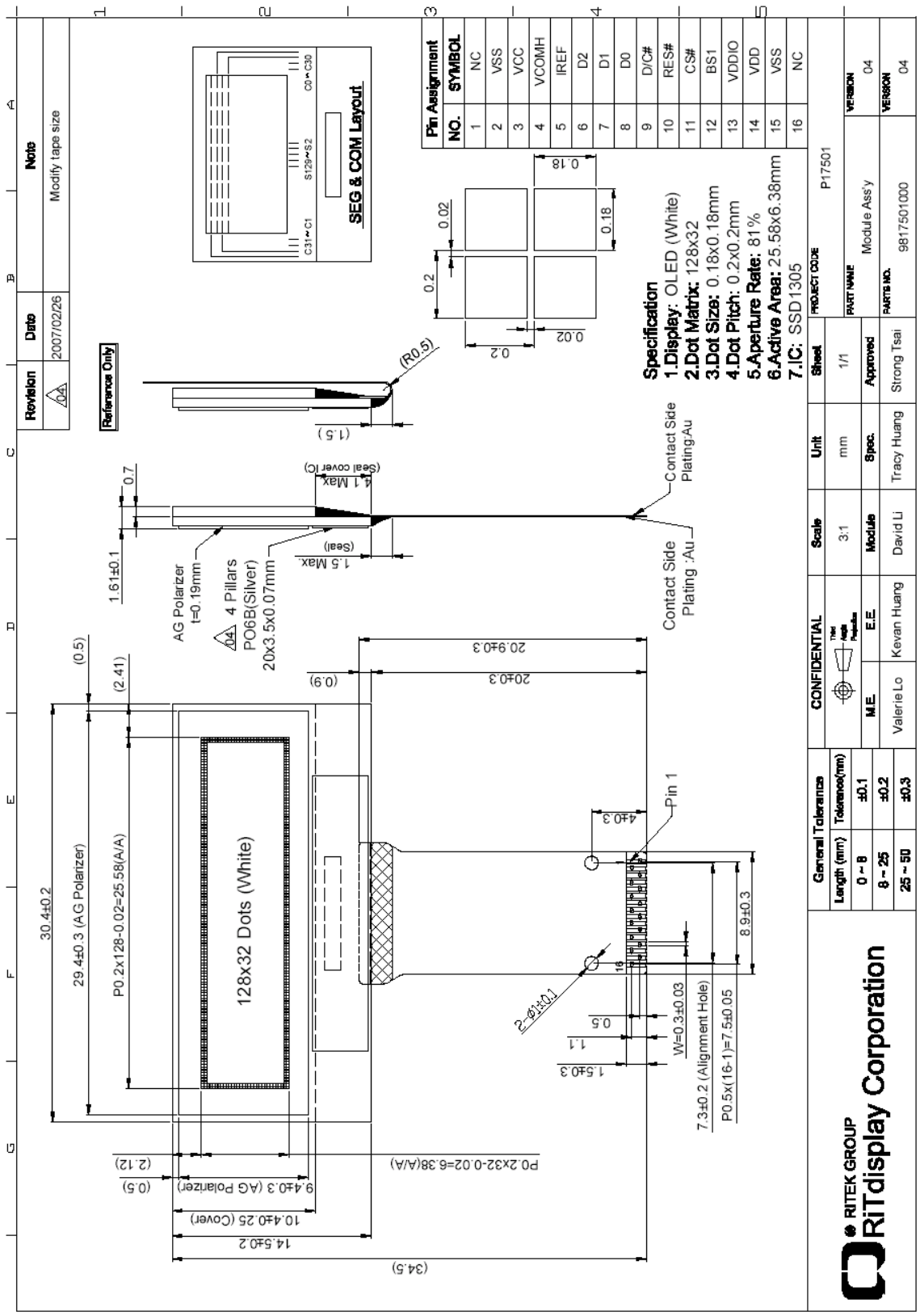
Test and measurement conditions

1. All measurements shall not be started until the specimens attain to temperature stability.
2. All-pixels-on is used as operation test pattern.
3. The degradation of Polarizer are ignored for item 1, 4 & 5.

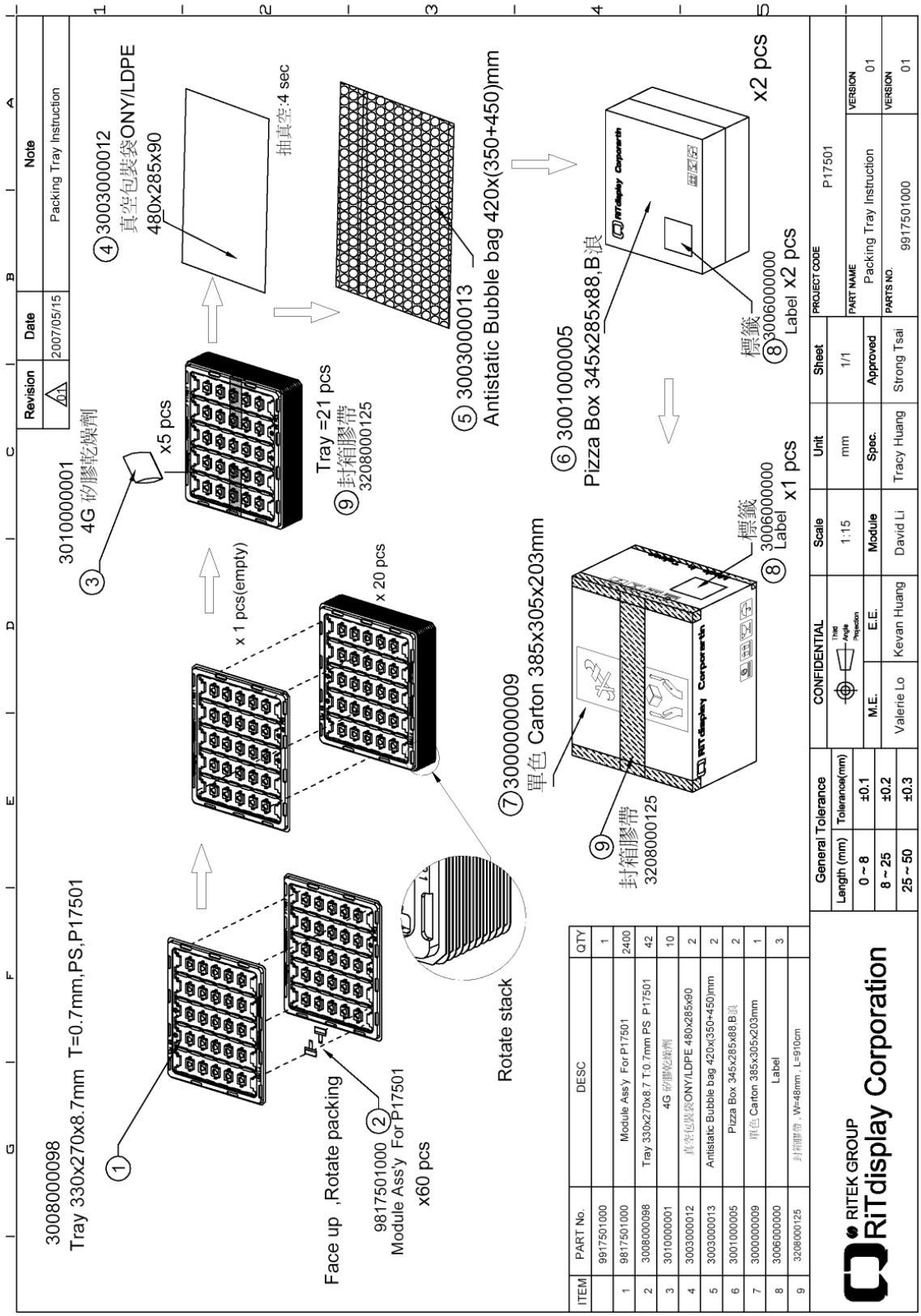
Evaluation criteria

1. The function test is OK.
2. No observable defects.
3. Luminance: > 50% of initial value.
4. Current consumption: within ± 50% of initial value.

10. EXTERNAL DIMENSION



11. PACKING SPECIFICATION



ITEM	PART No.	DESC	QTY
	9917501000		1
1	9817501000	Module Assy For P17501	2400
2	3008000098	Tray 330x270x8.7 T:0.7mm PS P17501	42
3	3010000001	4G 矽膠乾燥劑	10
4	3003000012	真空包裝袋ONY/LDPE 480x285x90	2
5	3003000013	Antistatic Bubble bag 420x(350+450)mm	2
6	3001000005	Pizza Box 345x285x88,B浪	2
7	3000000009	單色 Carton 385x305x203mm	1
8	3006000000	Label	3
9	3208000125	封箱膠帶, W=48mm, L=910cm	

12. APPENDIXES

APPENDIX 1: DEFINITIONS

A. DEFINITION OF CHROMATICITY COORDINATE

The chromaticity coordinate is defined as the coordinate value on the CIE 1931 color chart for R, G, B, W.

B. DEFINITION OF CONTRAST RATIO

The contrast ratio is defined as the following formula:

$$\text{Contrast Ratio} = \frac{\text{Luminance of all pixels on measurement}}{\text{Luminance of all pixels off measurement}}$$

C. DEFINITION OF RESPONSE TIME

The definition of turn-on response time Tr is the time interval between a pixel reaching 10% of steady state luminance and 90% of steady state luminance. The definition of turn-off response time Tf is the time interval between a pixel reaching 90% of steady state luminance and 10% of steady state luminance. It is shown in Figure 2.

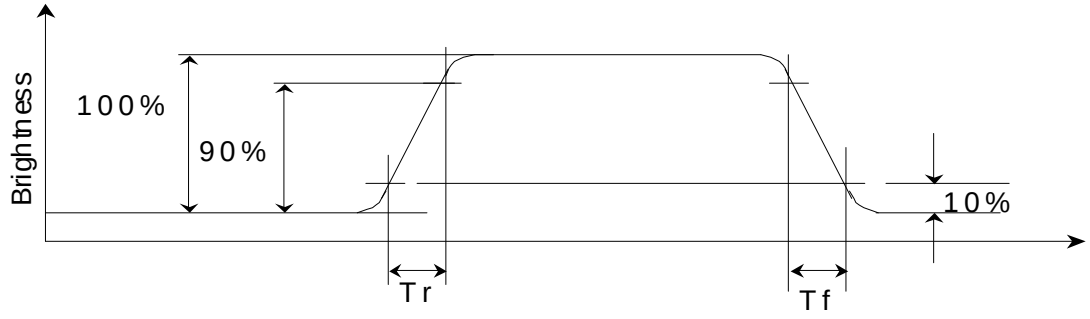


Figure 2: Response time

D. DEFINITION OF VIEWING ANGLE

The viewing angle is defined as Figure 3. Horizontal and vertical (H & V) angles are determined for viewing directions where luminance varies by 50% of the perpendicular value.

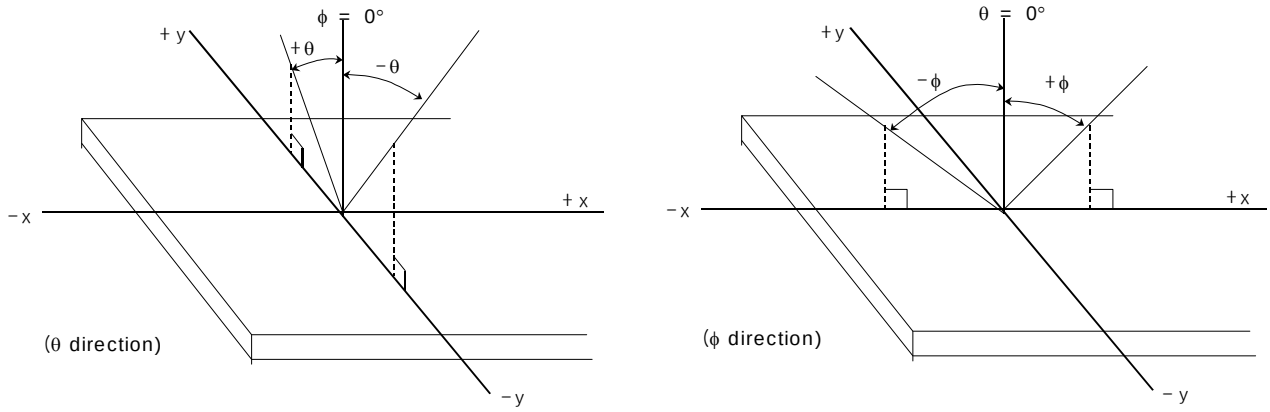
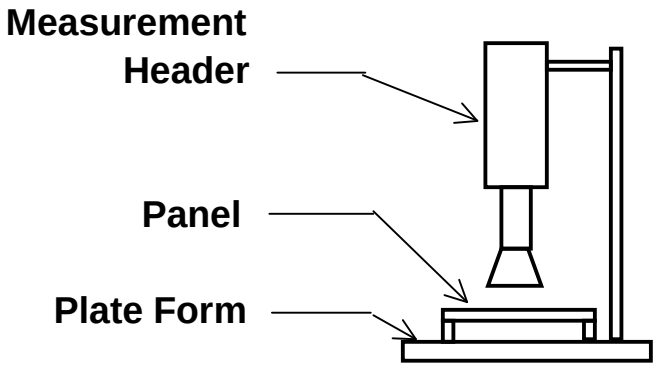


Figure 3: Viewing Angle

APPENDIX 2: MEASUREMENT APPARATUS

A. LUMINANCE/COLOR COORDINATE

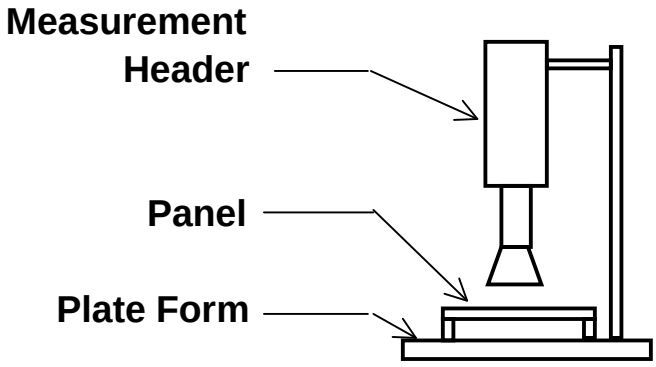
PHOTO RESEARCH PR-705, MINOLTA CS-100



**PR-705 /
MINOLTA CS-100
Color Analyzer**

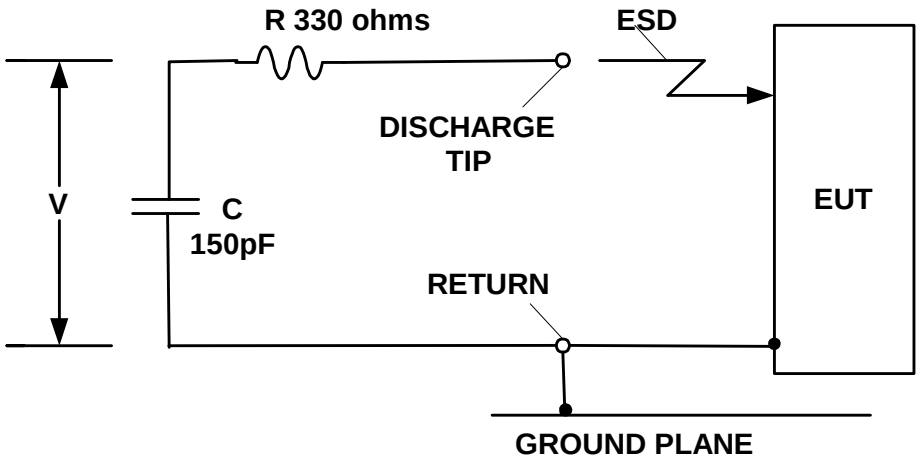
B. CONTRAST / RESPONSE TIME / VIEW ANGLE

WESTAR CORPORATION FPM-510



**Westar FPM-510
Display Contrast /
Response time /
View angle Analyzer**

C. ESD ON AIR DISCHARGE MODE



APPENDIX 3: PRECAUTIONS

A. RESIDUE IMAGE

Because the pixels are lighted in different time, the luminance of active pixels may reduce or differ from inactive pixels. Therefore, the residue image will occur. To avoid the residue image, every pixel needs to be lighted up uniformly.