Specification for Approval

PRODUCT NAME: **RGS10128032WR006**
PRODUCT NO.: **9923601000**

CUSTOMER
APPROVED BY
DATE:

RITDISPLAY CORP. APPROVED

REVISION RECORD

REV.	REVISION DESCRIPTION	REV. DATE	REMARK
X01	INITIAL RELEASE	2008. 12. 22	
X02	■ Add the operating conditions for different luminance ■ Modify the D.C electrical characteristics ■ Add the panel electrical specifications ■ Add the application circuit	2009. 02. 25	Page 6, 7, 8, 9 & 16
A01	■ Transfer from X version ■ Modify definition of panel thickness ■ Add the information of module weight ■ Add the packing specification	2009. 05. 13	Page 5 & 19

CONTENTS

ITEM	PAGE
1. SCOPE	4
2. WARRANTY	4
3. FEATURES	4
4. MECHANICAL DATA	5
5. MAXIMUM RATINGS	6
6. ELECTRICAL CHARACTERISTICS	7
6.1 D.C ELECTRICAL CHARACTERISTICS	
6.2 ELECTRO-OPTICAL CHARACTERISTICS	
7. INTERFACE	10
7.1 FUNCTION BLOCK DIAGRAM	
7.2 PANEL LAYOUT DIAGRAM	
7.3 PIN ASSIGNMENTS	
7.4 GRAPHIC DISPLAY DATA RAM ADDRESS MAP	
7.5 INTERFACE TIMING CHART	
8. POWER ON / OFF SEQUENCE & APPLICATION CIRCUIT	15
8.1 POWER ON / OFF SEQUENCE	
8.2 APPLICATION CIRCUIT	
8.3 COMMAND TABLE	
9. RELIABILITY TEST CONDITIONS	17
10. EXTERNAL DIMENSION	18
11. PACKING SPECIFICATION	19
12. APPENDIXES	20

1. SCOPE

The purpose of this specification is to define the general provisions and quality requirements that apply to the supply of display cells manufactured by RiTdisplay. This document, together with the Module Assembly Drawing, is the highest-level specification for this product. It describes the product, identifies supporting documents and contains specifications.

2. WARRANTY

RiTdisplay warrants that the products delivered pursuant to this specification (or order) will conform to the agreed specifications for twelve (12) months from the shipping date ("Warranty Period"). RiTdisplay is obligated to repair or replace the products which are found to be defective or inconsistent with the specifications during the Warranty Period without charge, on condition that the products are stored or used as the conditions specified in the specifications. Nevertheless, RiTdisplay is not obligated to repair or replace the products without charge if the defects or inconsistency are caused by the force majeure or the reckless behaviors of the customer.
After the Warranty Period, all repairs or replacements of the products are subject to charge.

3. FEATURES

- Small molecular organic light emitting diode.
- Color : White
- Panel matrix : 128*32
- Driver IC : LD7032
- Excellent quick response time.
- Extremely thin thickness for best mechanism design : 1.21mm
- High contrast : 2000:1
- Wide viewing angle : 160°
- 8080 or 6800 series parallel interface, Serial Peripheral Interface, I^2C Serial Interface.
- Wide range of operating temperature : -40 to 70 °C
- Anti-glare polarizer.

4. MECHANICAL DATA

NO	ITEM	SPECIFICATION	UNIT
1	Dot Matrix	128 (W) x 32 (H)	dot
2	Dot Size	0.18 (W) x 0.18 (H)	mm^2
3	Dot Pitch	0.20 (W) x 0.20 (H)	mm^2
4	Aperture Rate	81	%
5	Active Area	25.58 (W) x 6.38 (H)	mm^2
6	Panel Size	29.8 (W) x 15.4 (H)	mm^2
7*	Panel Thickness	1.02 ± 0.1	mm
8	Module Size	29.8 (W) x 22.4 (H) x 1.21 (D)	mm^3
9	Diagonal A/A size	1.0	inch
10	Module Weight	1.07 ± 10%	gram

* Panel thickness includes substrate glass, cover glass and UV glue thickness.

5. MAXIMUM RATINGS

ITEM	MIN	MAX	UNIT	Condition	Remark
Supply Voltage (VDD)	-0.3	3.63	V	-40～+85°C	IC maximum rating
Supply Voltage (VCC_C)	8	18	V	-40～+85°C	IC maximum rating
Operating Temp.	-40	70	°C		
Storage Temp	-40	85	°C		
Humidity	-	85	%		
Life Time	21,000	-	Hrs	140cd/m^2, 50% checkerboard	Note (1)
Life Time	25,000		Hrs	120 cd/m^2, 50% checkerboard	Note (2)
Life Time	30,000	-	Hrs	100 cd/m^2, 50% checkerboard	Note (3)

Note:

(A) Under VCC_C = 12V, Ta = 25°C, 50% RH.

(B) Life time is defined the amount of time when the luminance has decayed to less than 50% of the initial measured luminance.

(C) Note (1)、Note (2)、Note (3) contrast setting are under VDD = 2.8V, set VDD selection(0x3d)=(0x00) and VDD = 1.8V, set VDD selection(0x3d)=(0x01).

(1) Setting of 140 cd/m^2 :

- Contrast setting : 0x48
- Frame rate : 105Hz
- Duty setting : 1/32

(2) Setting of 120 cd/m^2 :

- Contrast setting : 0x3d
- Frame rate : 105Hz
- Duty setting : 1/32

(3) Setting of 100 cd/m^2 :

- Contrast setting : 0x34
- Frame rate : 105Hz
- Duty setting : 1/32

6. ELECTRICAL CHARACTERISTICS

6.1 D.C ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNIT
VDD	Logic Power 1		1.65	1.8 2.8	3.5	V
VCC_C	OLED operating voltage		11.5	12	12.5	V
V_{IH}	High Logic Input Level		0.8*VDD	-	VDD	V
V_{IL}	Low Logic Input Level		0	-	0.2*VDD	V
V_{OH}	High Logic Output Level	Iout＝-100uA	0.9*VDD	-	VDD	V
V_{OL}	Low Logic Output Level	Iout＝100uA	0	-	0.1*VDD	V
IIL	Input Leakage Current		－1.0		+1.0	μA
IRVCC	VCC_R Power Regulator Output Voltage	VCC_R = 0.8*VCC_C I_{VCC_R}=5mA	0.75* VCC_C	0.8* VCC_C	0.85* VCC_C	V

6.2 ELECTRO-OPTICAL CHARACTERISTICS

PANEL ELECTRICAL SPECIFICATIONS

PARAMETER	MIN	TYP.	MAX	UNITS	COMMENTS
Normal mode current		7	8	mA	All pixels on (1)
Standby mode current		2	3	mA	Standby mode 10% pixels on (2)
Normal mode power consumption		84	96	mW	All pixels on (1)
Standby mode power consumption		24	36	mW	Standby mode 10% pixels on (2)
Normal Luminance	100	120		cd/m^2	Display Average
Standby Luminance		30		cd/m^2	Display Average
CIEx (White)	0.24	0.28	0.32		x, y (CIE 1931)
CIEy (White)	0.28	0.32	0.36		
Dark Room Contrast	2000:1				
Viewing Angle	160			degree	
Response Time		10		μs	

Note: While VDD is 2.8V, set VDD selection(0x3d)=(0x00) ,VDD is 1.8V, set VDD selection(0x3d)=(0x01) contrast setting is shown below.

(1) Normal mode condition :

- Driving Voltage : 12V
- Contrast setting : 0x3d
- Frame rate : 105Hz
- Duty setting : 1/32

(2) Standby mode condition :

- Driving Voltage : 12V
- Contrast setting : 0x14
- Frame rate : 105Hz
- Duty setting : 1/32

VDD(Analog and digital voltage supply):1.8V、2.8V、3.3V Setting

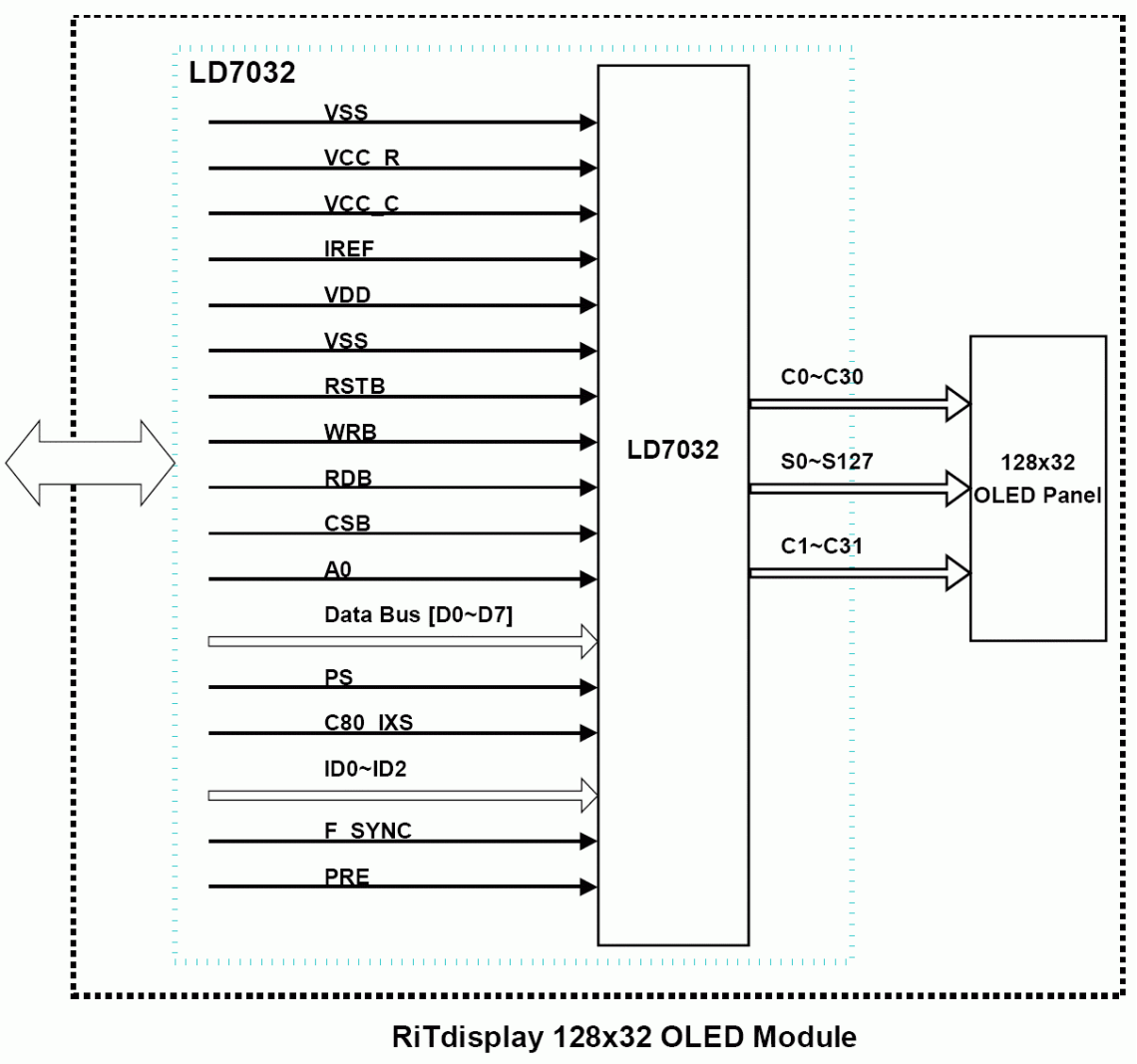
Brightness(cd/m^2)	VDD(V)	Set VDD Selection (0x3d)	Dot Matrix Current Level (0x12)
30(Standby mode)	1.8	0x01	0x14
100(minimum mode)	1.8	0x01	0x34
120(Typical mode)	1.8	0x01	0x3d
140(Maximum mode)	1.8	0x01	0x48

Brightness(cd/m^2)	VDD(V)	Set VDD Selection (0x3d)	Dot Matrix Current Level (0x12)
30(Standby mode)	2.8	0x00	0x14
100(minimum mode)	2.8	0x00	0x34
120(Typical mode)	2.8	0x00	0x3d
140(Maximum mode)	2.8	0x00	0x48

Brightness(cd/m^2)	VDD(V)	Set VDD Selection (0x3d)	Dot Matrix Current Level (0x12)
30(Standby mode)	3.3	0x00	0x11
100(minimum mode)	3.3	0x00	0x2e
120(Typical mode)	3.3	0x00	0x36
140(Maximum mode)	3.3	0x00	0x40

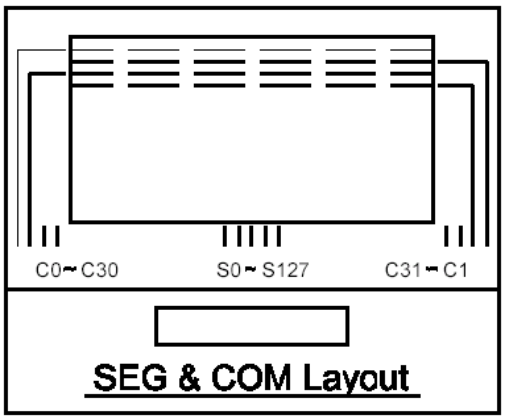
7. INTERFACE

7.1 FUNCTION BLOCK DIAGRAM



RiTdisplay 128x32 OLED Module

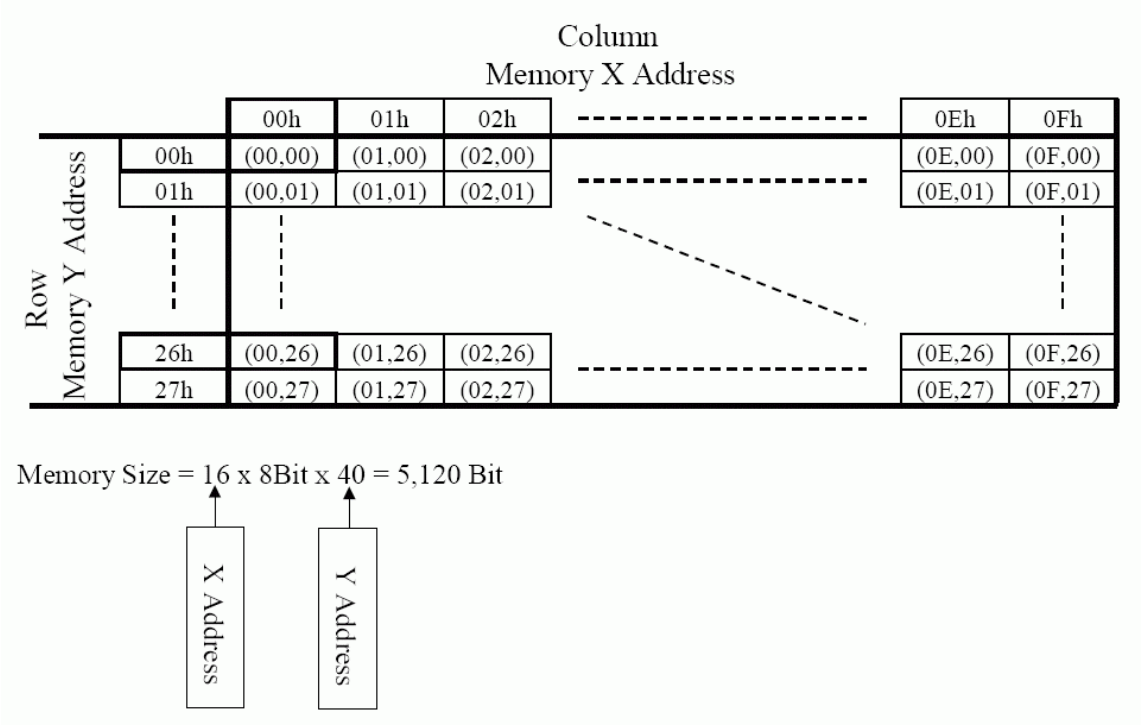
7.2 PANEL LAYOUT DIAGRAM



7.3 PIN ASSIGNMENTS

PIN NO.	PIN NAME	DESCRIPTION
1	VSS	Ground pin.
2	VCC_R	OELD Dot Matrix Power Supply for Row Driver. A 4.7uF capacitor is recommended to connect between VCC_R and GND. If internal row power regulator is disabled, It must be connected to the external high voltage source or VCC_C.
3	VCC_C	OELD Dot Matrix Power Supply for Column VCC_C Driver.
4	IREF	This pin is the dot output current reference pin. A resister should be connected between this pin and VSS.
5	VDD	Analog and digital voltage supply.
6	VSS	Ground pin.
7	RSTB	Reset (Active Low).
8	WRB	Write (Active Low, 80 Interface). H:Read L:Write (68 Interface).
9	RDB	Read (Active Low, 80 Interface). Enable (68 Interface).
10	CSB	Chip Select (Active Low).
11	A0	Address (L: command, H: Parameter).
12	D7	These are 8-bit bi-directional data bus to be connected to the microprocessor's data bus. When I^2C interface mode is selected, D1 will be the I^2C data input (SDA) and D0 will be the I^2C bus clock input (SCL), and D2 ~ D7 should be tied VDD or VSS or floating. When serial interface mode is selected, D1 will be the serial data input (SDIN), D0 will be the serial clock input (SCLK), and D2 ~ D7 should be tied VDD or VSS or floating.
13	D6	
14	D5	
15	D4	
16	D3	
17	D2	
18	D1	
19	D0	
20	PS	H: Parallel L: Serial
21	C80_IXS	H: 68CPU, I^2C is selected. L: 80CPU, I^2C is not selected.
22	ID2	These pins configure I^2C interface address. Using these pins, I^2C Address can be selected.
23	ID1	
24	ID0	
25	F_SYNC	Frame Sync Signal.
26	PRE	Pre-Charge Voltage.
27	VCC_C	OELD Dot Matrix Power Supply for Column VCC_C Driver.
28	VSS	Ground pin.

7.4 GRAPHIC DISPLAY DATA RAM ADDRESS MAP

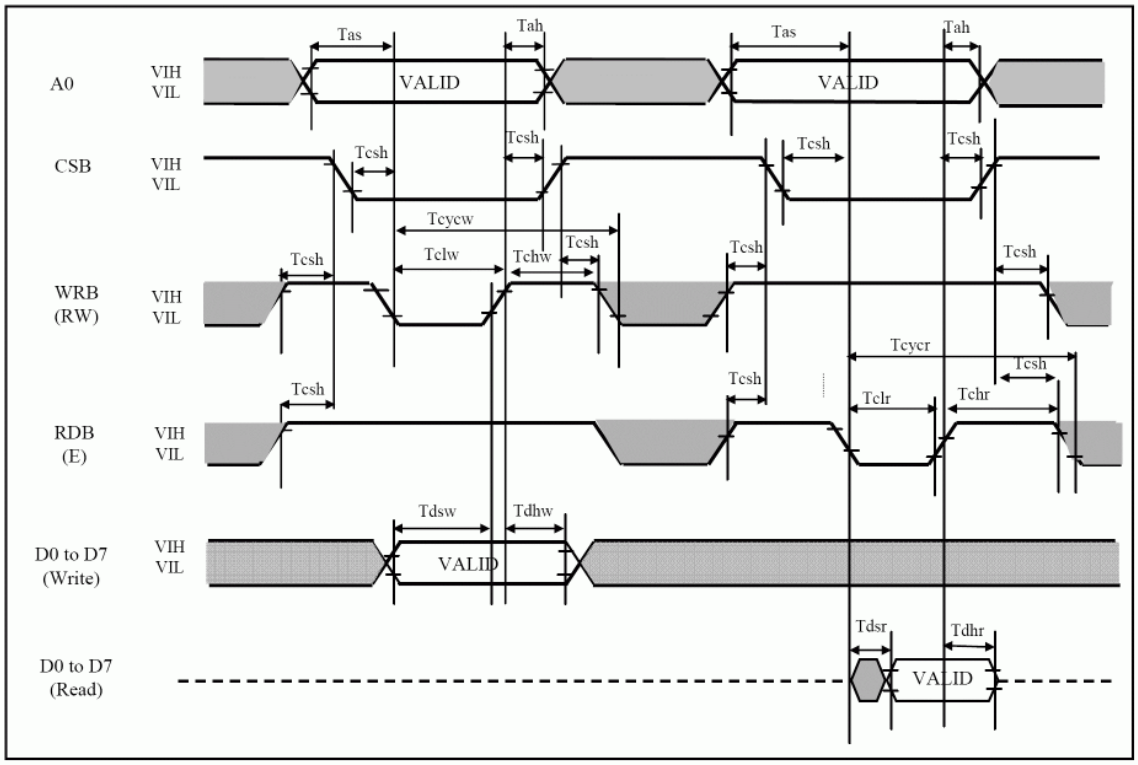


7.5 INTERFACE TIMING CHART

Parallel Interface1 (Write/Read Timing)

(VSS = 0V, VDD= 2.6V~3.5V, Ta = 25℃)

Parameter	Symbol	Condition		Specification MIN	Specification MAX	Units
Address setup time	Tas	A0		20		ns
Address hold time	Tah	A0		10		
System cycle time	Tcycw	WRB	Write	100		
	Tcycr	RDB	Read	500		
Write control low pulse width	Tclw	WRB		40		
Write control high pulse width	Tchw			40		
Read control low pulse time	Tclr	RDB		60		
Read control high pulse time	Tchr			80		
Write data setup time	Tdsw	D0 – D7		20		
Write data hold time	Tdhw			10		
Read data setup time (Data Output Access Time)	Tdsr				200	
Read data hold time (Data output disable time)	Tdhr			10		
CSB – WRB , RDB time	Tcsh	CSB		10		



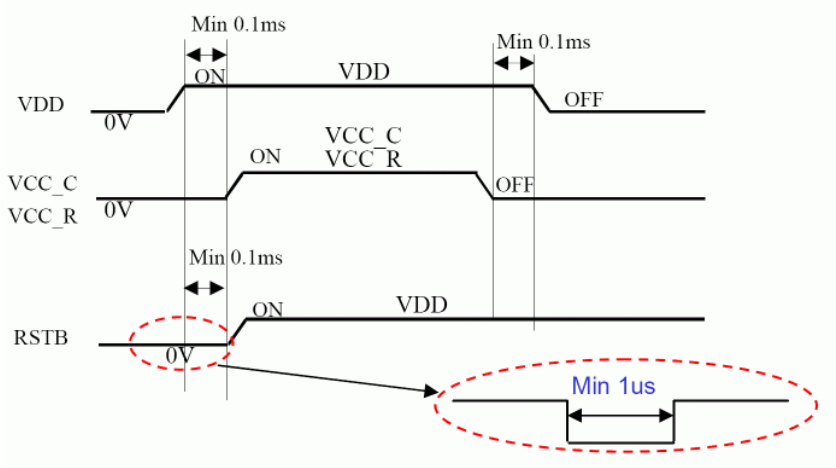
Parallel Interface2 (Write/Read Timing)

(VSS = 0V, VDD= 1.65V~3.5V, Ta = 25℃)

Parameter	Symbol	Condition		Specification		Units
				MIN	MAX	
Address setup time	Tas	A0		60		ns
Address hold time	Tah	A0		30		
System cycle time	Tcycw	WRB	Write	300		
	Tcycr	RDB	Read	500		
Write control low pulse width	Tclw	WRB		120		
Write control high pulse width	Tchw			120		
Read control low pulse time	Tclr	RDB		60		
Read control high pulse time	Tchr			80		
Write data setup time	Tdsw	D0 – D7		60		
Write data hold time	Tdhw			30		
Read data setup time (Data Output Access Time)	Tdsr				200	
Read data hold time (Data output disable time)	Tdhr			10		
CSB – WRB , RDB time	Tcsh	CSB		30		

8. POWER ON / OFF SEQUENCE & APPLICATION CIRCUIT

8.1 POWER ON / OFF SEQUENCE



Power On Sequence

System Power On 1 (Vdd On)

Wait for Several ms

RESB Active

System Power On 2 (Vcc On)

Wait for Several ms

Use Graphics Case

DSTBY OFF 14h 00h

3.Panel Condition Set

4.Drive Condition Set

5.Memory Data Write

DDISP ON 02h 01h

Graphics Off Sequence

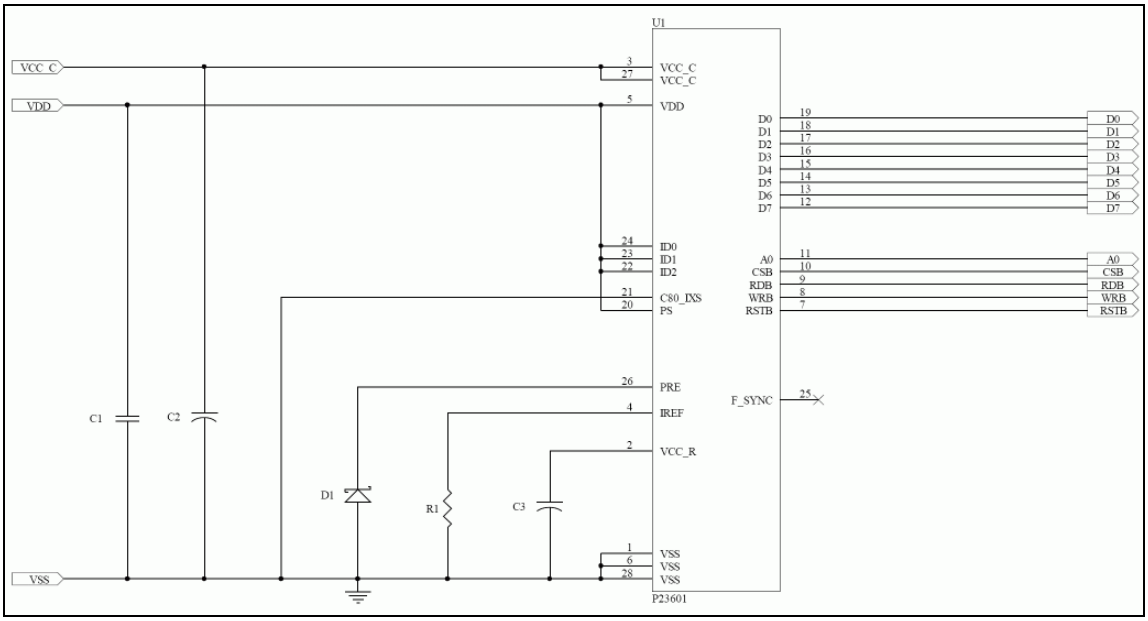
Iref Off	12h 00h
DDISP Off	02h 00h
DSTBY ON	14h 01h

System Power Off 2 (Vcc Off)

Wait for Several ms

System Power Off 1 (Vdd Off)

8.2 APPLICATION CIRCUIT



Recommend components:

C1: 1uF/16V(0603)

C2, C3: 4.7uF/35V (Tantalum type) or VISHAY (572D475X0025A2T)

R1: 68K ohm (0603) 1%

D1: UDZSTE-172.7B or PDZ2.7B (zener diode)

This circuit is for 8080 8bits interface.

8.3 COMMAND TABLE

Refer to LD7032 IC Spec.

9. RELIABILITY TEST CONDITIONS

No.	Items	Specification	Quantity
1	High temp. (Non-operation)	85°C, 240hrs	5
2	High temp. (Operation)	70°C, 120hrs	5
3	Low temp. (Operation)	-40°C, 120hrs	5
4	High temp. / High humidity (Operation)	65°C, 90%RH, 120hrs	5
5	Thermal shock (Non-operation)	-40°C ~85°C (-40°C /30min; transit /3min; 85°C /30min; transit /3min) 1cycle: 66min, 100 cycles	5
6	Vibration	Frequency : 5~50HZ, 0.5G Scan rate : 1 oct/min Time : 2 hrs/axis Test axis : X, Y, Z	1 Carton
7	Drop	Height: 120cm Sequence : 1 angle、3 edges and 6 faces Cycles: 1	1 Carton
8	ESD (Non-operation)	Air discharge model, ±8kV, 10 times	5

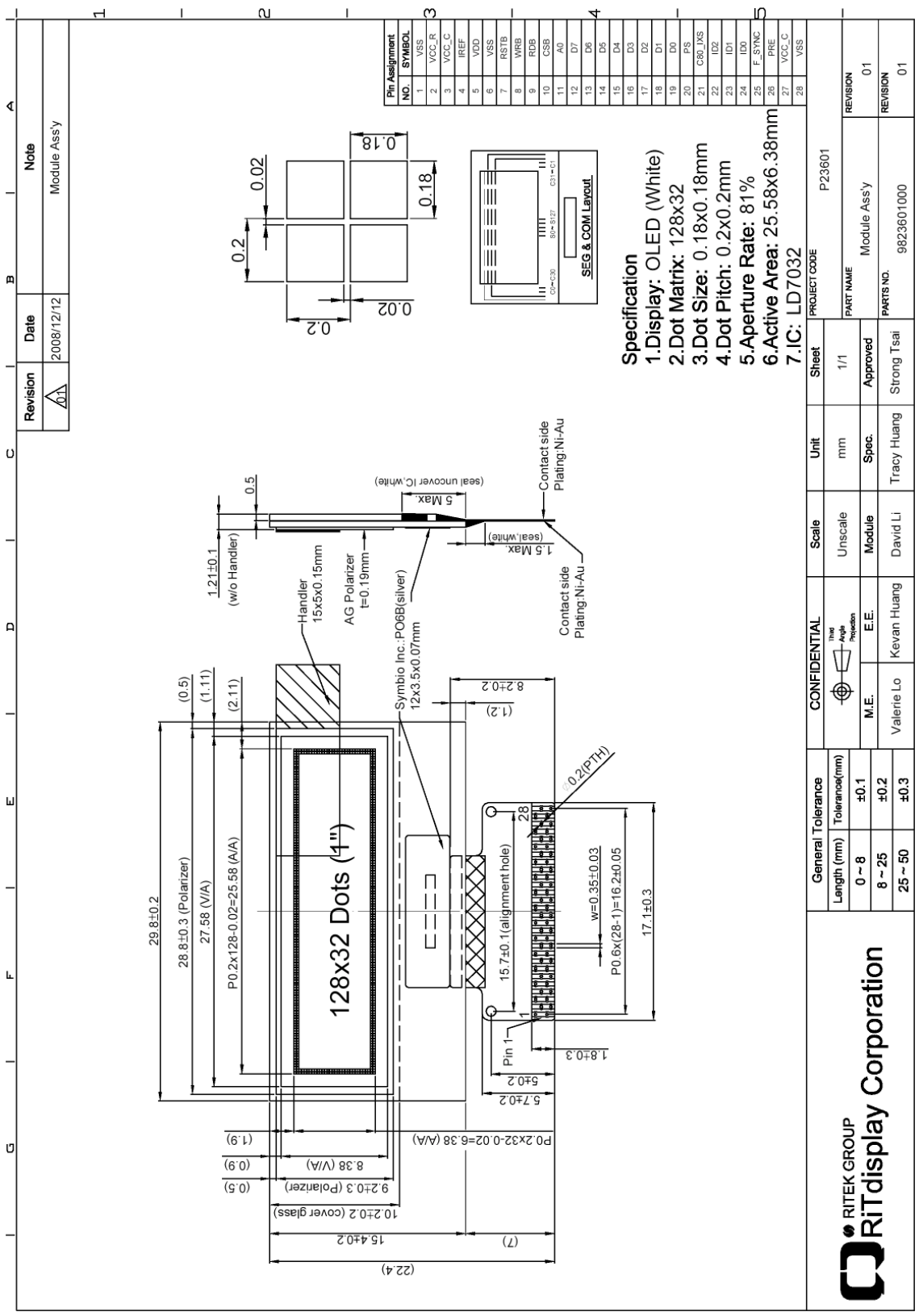
Test and measurement conditions

1. All measurements shall not be started until the specimens attain to temperature stability.
2. All-pixels-on is used as operation test pattern.
3. The degradation of Polarize are ignored for item 1, 4 & 5.

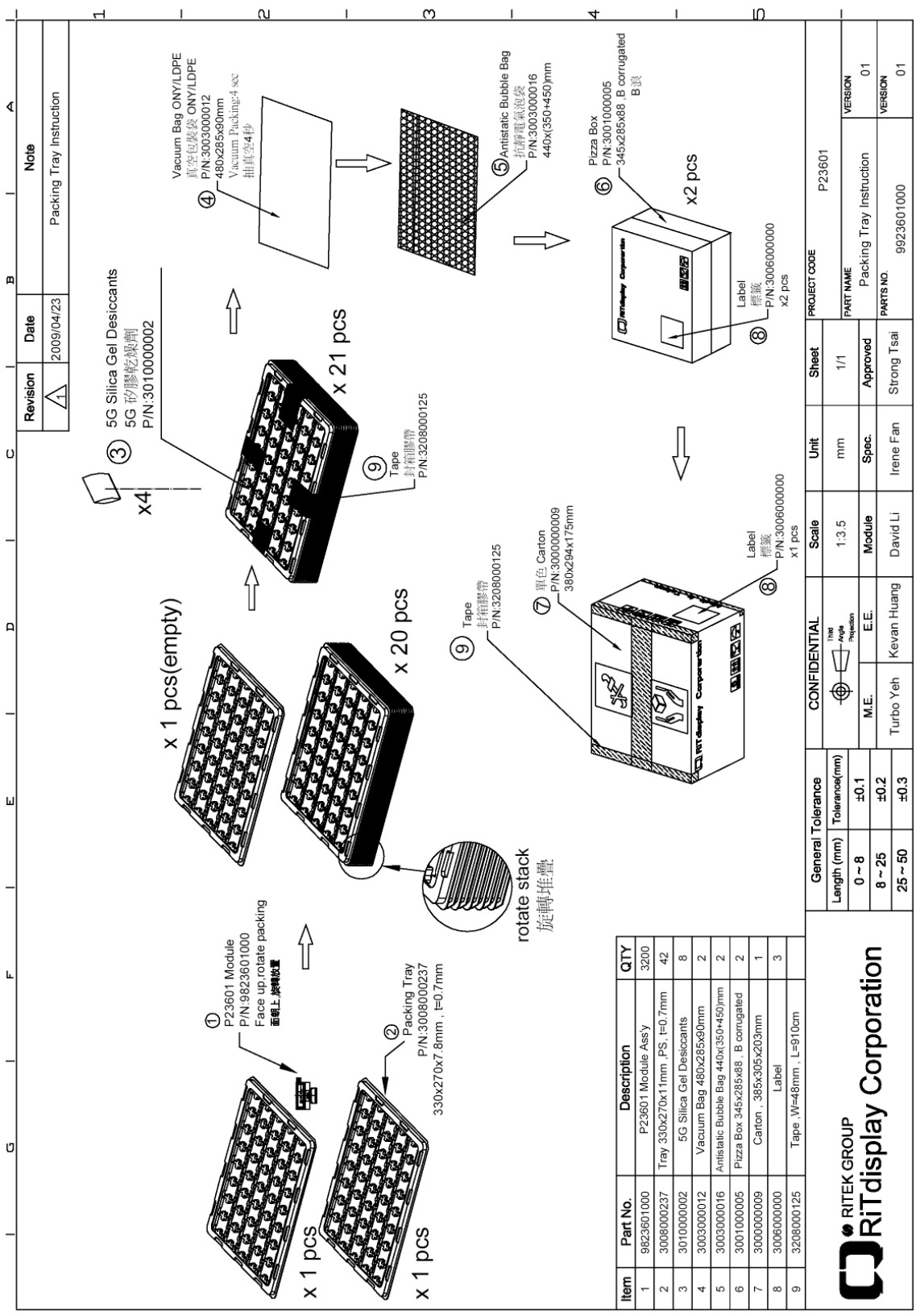
Evaluation criteria

1. The function test is OK.
2. No observable defects.
3. Luminance: > 50% of initial value.
4. Current consumption: within ± 50% of initial value.

10. EXTERNAL DIMENSION



11. PACKING SPECIFICATION



12. APPENDIXES

APPENDIX 1: DEFINITIONS

A. DEFINITION OF CHROMATICITY COORDINATE

The chromaticity coordinate is defined as the coordinate value on the CIE 1931 color chart for R, G, B, W.

B. DEFINITION OF CONTRAST RATIO

The contrast ratio is defined as the following formula:

$$\text{Contrast Ratio} = \frac{\text{Luminance of all pixels on measurement}}{\text{Luminance of all pixels off measurement}}$$

C. DEFINITION OF RESPONSE TIME

The definition of turn-on response time Tr is the time interval between a pixel reaching 10% of steady state luminance and 90% of steady state luminance. The definition of turn-off response time Tf is the time interval between a pixel reaching 90% of steady state luminance and 10% of steady state luminance. It is shown in Figure 2.

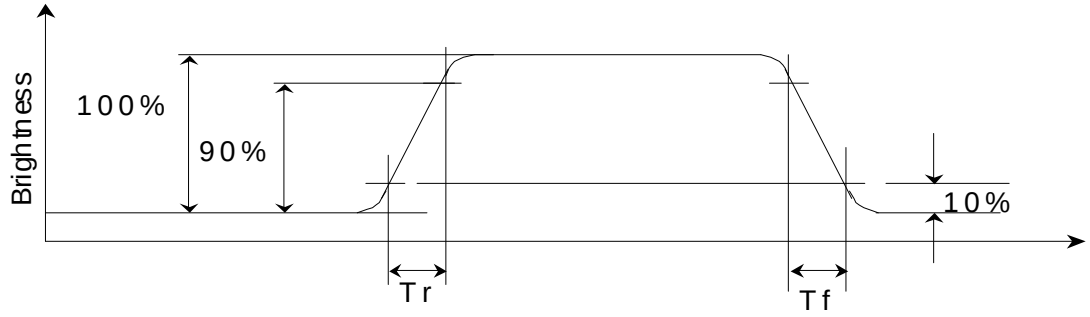


Figure 2: Response time

D. DEFINITION OF VIEWING ANGLE

The viewing angle is defined as Figure 3. Horizontal and vertical (H & V) angles are determined for viewing directions where luminance varies by 50% of the perpendicular value.

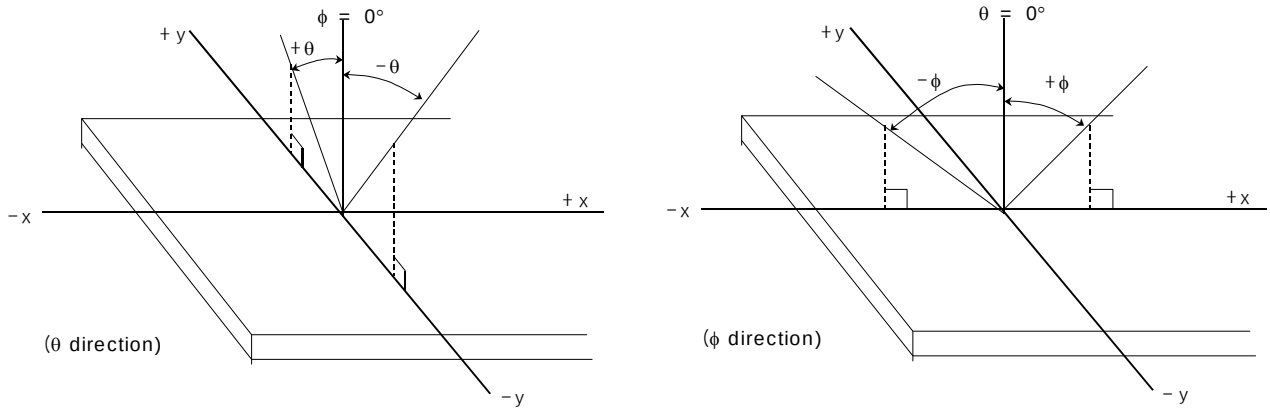


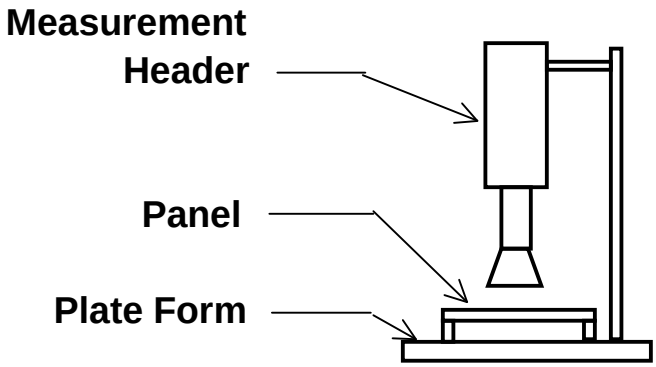
Figure 3: Viewing Angle

REV.: A01 2009/05/13

APPENDIX 2: MEASUREMENT APPARATUS

A. LUMINANCE/COLOR COORDINATE

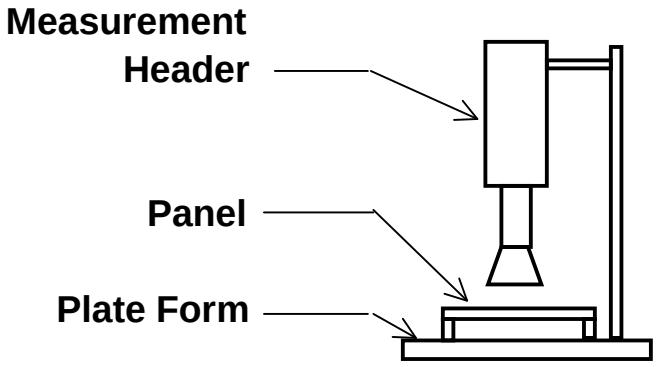
PHOTO RESEARCH PR-705, MINOLTA CS-100



**PR-705 /
MINOLTA CS-100
Color Analyzer**

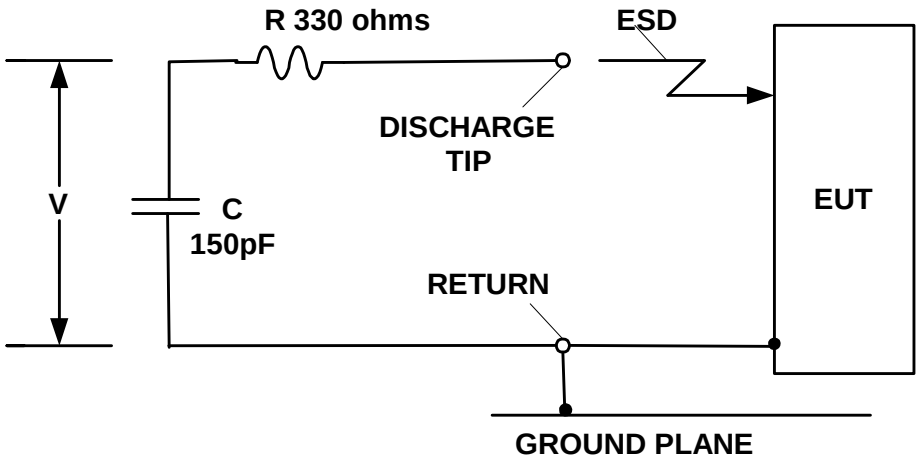
B. CONTRAST / RESPONSE TIME / VIEW ANGLE

WESTAR CORPORATION FPM-510



**Westar FPM-510
Display Contrast /
Response time /
View angle Analyzer**

C. ESD ON AIR DISCHARGE MODE



APPENDIX 3: PRECAUTIONS

A. RESIDUE IMAGE

Because the pixels are lighted in different time, the luminance of active pixels may reduce or differ from inactive pixels. Therefore, the residue image will occur. To avoid the residue image, every pixel needs to be lighted up uniformly.